Appendix D - Data Sheets Of Key Components

- E2580 EML Agere
  Application Notes
- LTC1923 TEC controller Linear Technology
  Application Notes
- HY6330 Laser Diode Driver Hytek
- MAX525 Digital to Analog Converter Maxim
- ADS7841 Analog to Digital Converter Burr Brown Products (TI)
- MAX 487 RS422 Transceiver Maxim

E2580 EML with Intergral Driver IC: Pin Definitions and Operation

Introduction

Agere Systems Inc.'s E2580 series Electroabsorption Modulated Isolated Laser Module (EM-ILM or EML) offers an integrated modulator and CW laser in a single semiconductor chip, and an integral driver IC in the same package.

This application note is intended to offer guidance on the pin functions and the voltage levels required by the driver IC. For general guidance in setup and operation of EML devices, refer to the *Electroabsorptive Modulated Laser (EML): Setup and Optimization* Technical Note (TN00-008OPTO). For additional information on the wavelength stability of 2.5 Gbits/s and 10 Gbits/s EML devices over temperature, refer to the technical note, *Use of EML Devices In DWDM Applications* (TN00-012OPTO).

Pin Definitions and Operation

As indicated in the block diagram below, the E2580 device has 13 pins on one side of the package that are dedicated to the required dc and control components, and a single, small-profile, Glibert GPO connector on the other side for the RF signal. Pins 6 to 11 interface to the integral driver IC, which in turn controls the modulator functions. Pins 1 and 2 connect the thermistor, pin 3 connects the CW laser section, pins 4 and 5 connect the monitor photodiode, and pins 12 and 13 connect the thermoelectric cooler.

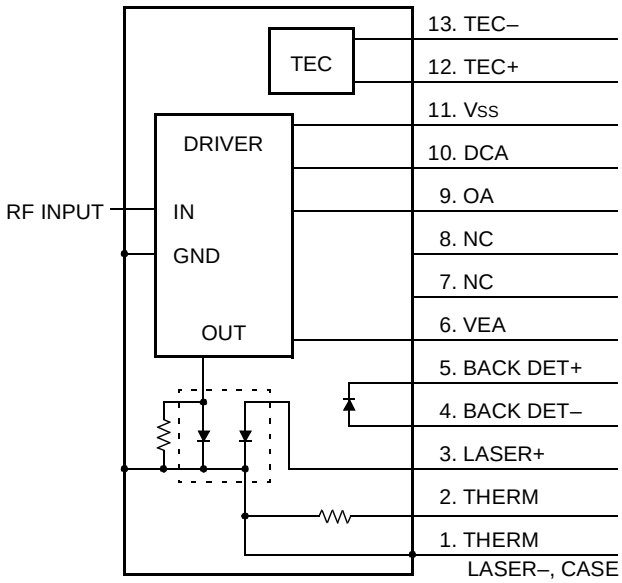

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Figure 1. Block Diagram of the E2580 10 Gbits/s EML Package with Driver IC and Output Amplitude/Cross Point Control Circuits

Pin Definitions and Operation (continued)

Table 1. Pin Definitions and Operation

PIn Number	Symbol	Description
13	TEC(–)	**Thermoelectric Cooler (–).**
12	TEC(+)	**Thermoelectric Cooler (+).**
11	V_{SS}	**Voltage Supply to the IC.** The operating voltage range is –5.0 V to –5.5 V.
10	DCA	**Duty Cycle Adjust.** The input range is ~ –3.6 V to –3.8 V. At ~ –3.6 V, the pulse width is reduced to a minimum value of 70%. At ~ –3.8 V, the pulse width is a maximum at 130%. Typically, around –3.7 V, the pulse width is 100%, which corresponds to a normal duty cycle and 50% eye crossing for the electrical drive pattern. This will produce lower eye crossings in the optical pattern for an EML device because of the nonlinear extinction (light output vs. modulation voltage) characteristic. This input can be used to increase the crossings slightly for optimal performance.
9	OA	**Output Amplitude Adjust.** The input range is ~ –4.2 V to –4.8 V. Minimum drive amplitude to the modulator (~ 2 Vp-p) is achieved at –4.8 V. Maximum drive (~ 3 Vp-p) is attained at –4.2 V. This input can be used to adjust the extinction ratio in the optical output.
8	NC/DCM	**No Connect/Duty Cycle Monitor**. This pin is reserved for the duty cycle monitor function and may be available in future transponder versions. Currently, this functionality is not available on the driver ICs that are used in E2560. It will be NC, (no connect) on initial models.
7	NC/PCM	**No Connect/Peak Current Monitor.** This pin is reserved for the peak current monitor function. As with the duty cycle monitor, it is not yet available on the driver ICs used. It will be NC (no connect) on initial models
6	VEA	**Modulator Offset**. This pin controls the on-state bias voltage applied to the modulator. The input voltage ranges from –3.0 V to –5.0 V. At –5.0 V, there is no applied offset to the modulator, i.e., the on-state should be close to 0.0 V (excluding the effects of modulator photocurrent). At –3.0 V, the maximum offset is applied to the modulator, which would correspond to an on-state voltage of –1.0 V. The absolute minimum off-state is –3.4 V for the driver IC. Therefore, tuning the offset to more negative value at a fixed output amplitude will eventually result in clipping on the low end and a reduction in the drive amplitude. For example, if a package is set up for 2.5 Vp-p output amplitude, it may be tuned down for offset to –0.9 V maximum before amplitude clipping would normally occur. At –1.0 V offset, the maximum driver amplitude would be reduced to 2.4 Vp-p.
5	Back Det(+)	**Back Detector (+) (Cathode).**
4	Back Det(–)	**Back Detector (–) (Anode).**
3	Laser(+)	**Laser (+) (Anode).**
2	Therm	**Thermistor Connect.**
1	Therm/Laser(–)/Case	**Thermistor/Laser (–)/Case.**This pin offers a combined thermistor, laser CW section cathode (–) and case ground (for the RF signal). This is a modification on earlier models and has been introduced to offer optimum RF performance.
—	RF_{IN}	**RF Input.** The RF signal is applied to the Gilbert GPO connector. Via this connection, the driver IC requires an input voltage in the range 0.5 V to 1.0 V (peak to peak) for optimum performance. The RF path is optimized for a nominal input impedance of 50 Ω.

Pin Definitions and Operation (continued)

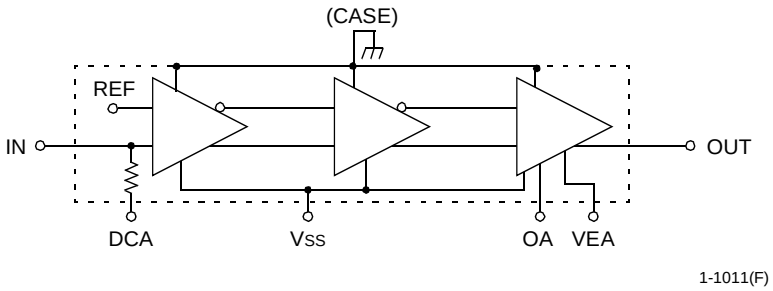


Figure 2. Driver IC Block Diagram

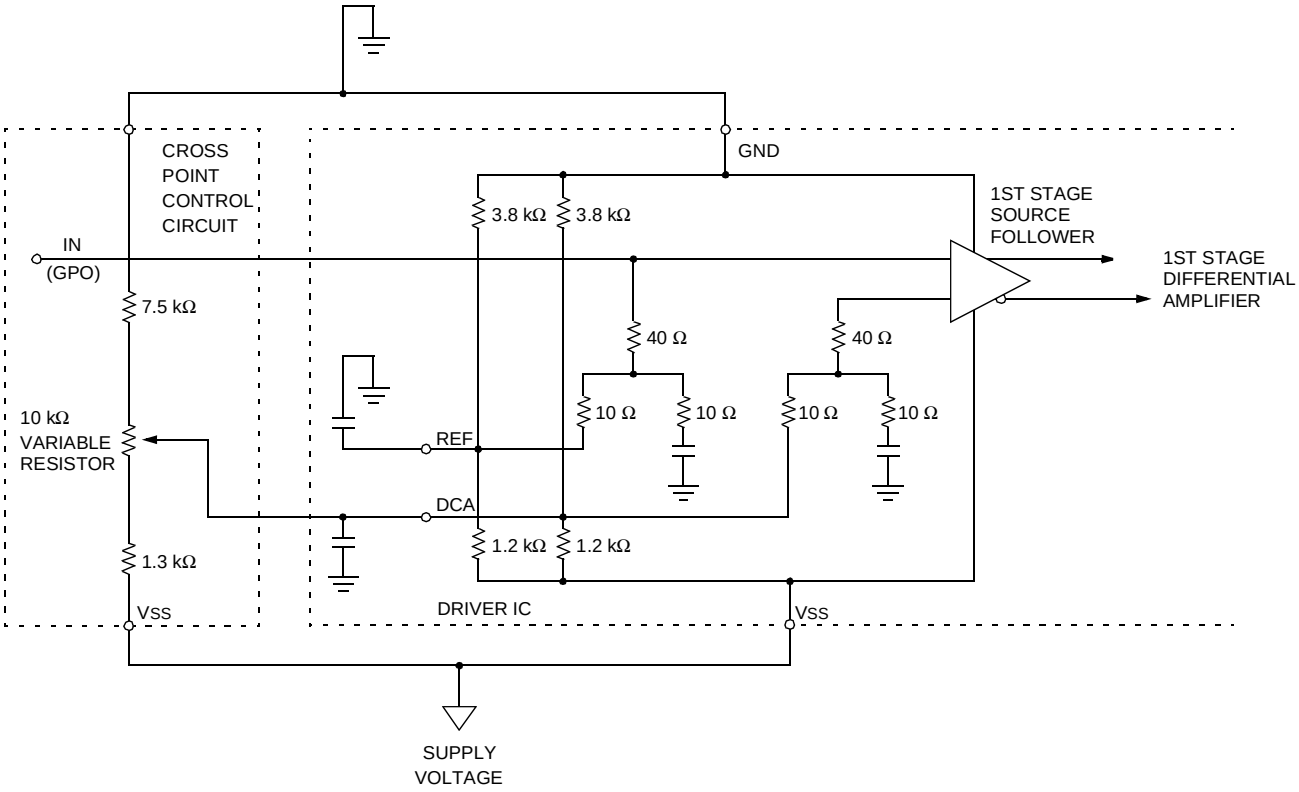


Figure 3. Cross Point Control Circuit Example

Pin Definitions and Operation (continued)

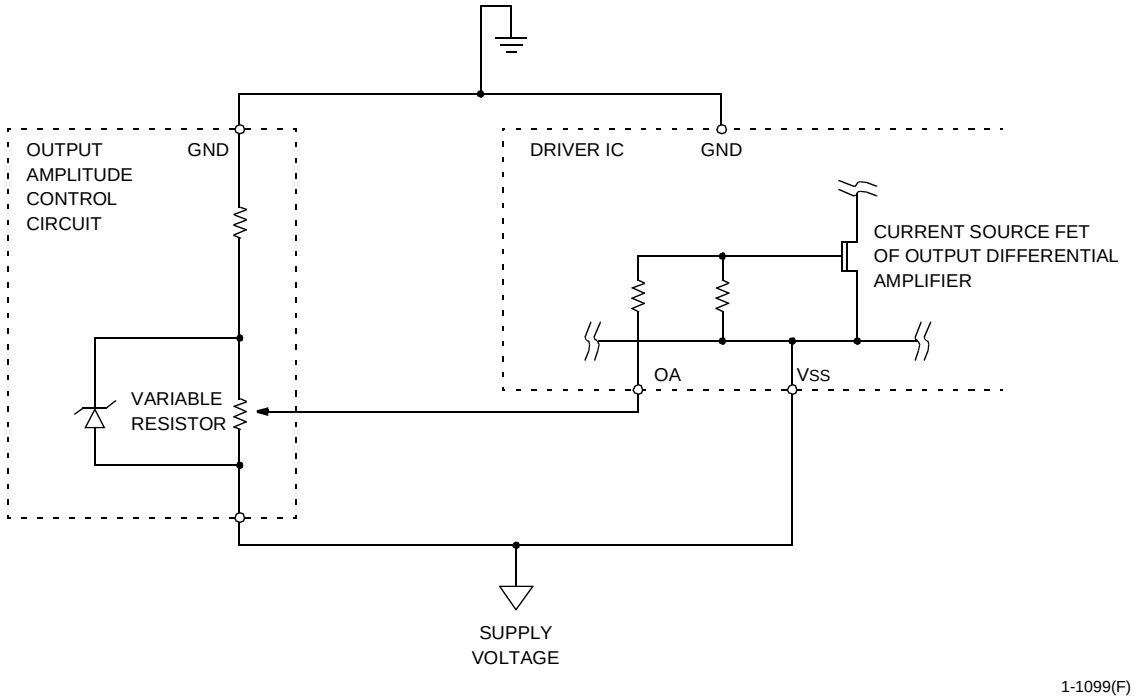


Figure 4. Output Amplitude Control Circuit Example (10 Gbits/s EA Driver IC)

Recommended Start-Point Conditions

With the appropriate control circuits in place, as described above, the following starting point (i.e., prior to any tuning) values are suggested for the dc bias parameters in the IC.

Table 2. Recommended Start-point Conditions for dc Bias Parameters in the IC*

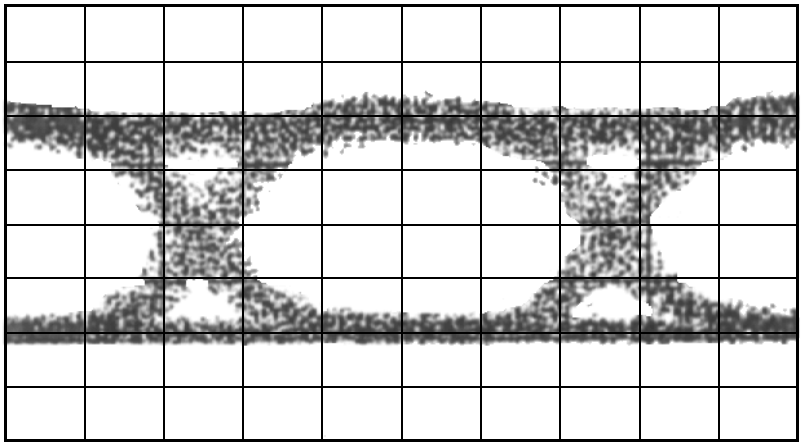
Parameter	Symbol	Value
Duty Cycle Adjust	DCA	–3.7 ± 0.1 V
Modulation Offset	VEA	–3.5 ± 0.3 V
Output Amplitude	OA	–4.6 ± 0.2 V

* The information offered here is recommended as a time-saving condition and further adjustment may be necessary to achieve the desired performance, as described in Table 1.

Summary

In conjunction with the technical note describing general setup and optimization of the EML device, the user should now be in a position to design the interface to the E2580 package, and, subsequently, to optimize its performance to meet the individual system requirements.

Appendix



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RISE TIME = 37 ps, FALL TIME = 40 ps.

Figure 5. E2580xx Eye Pattern (Example)

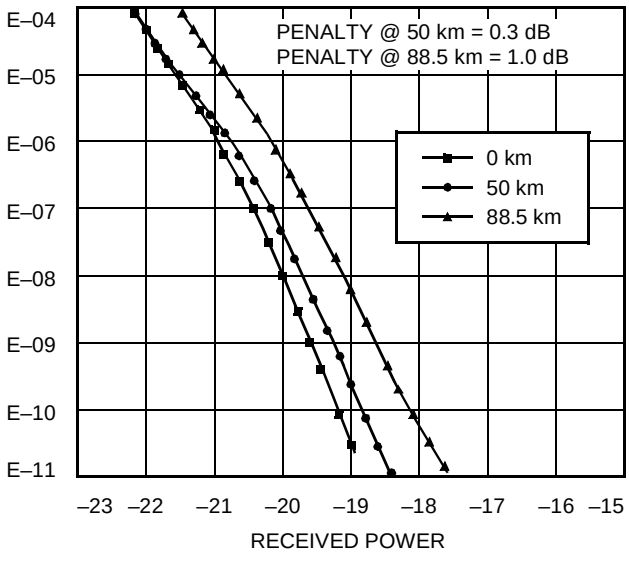

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Figure 6. E2581xx BER Performance (Example)

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May 2000
AP00-023OPTO

agere systems

Technical Note
August 2000

Using Electroabsorbtive Modulated Laser Modules in Dense WDM Applications

Introduction

The information offered here is intended to serve as a guide in the use and optimization of Agere Systems Inc.' E2500 series of 2.5 Gbits/s and 10 Gbits/s Electroabsorptive Modulated Isolated Laser Module (EM-ILM, or EML) in dense wave-division multiplexing (DWDM) systems, where performance over temperature and, in particular, wavelength aging over life need to be characterized and understood. Use of the device without the introduction of a wavelength-locking element is discussed. Use of wavelength stabilized devices (e.g., Agere Systems' C488/489-Type transmitters that employ an integrated wavelength locker) are not covered by this document.

For general notes on the use of EML devices in long and ultralong haul transmission applications, refer to the *Electroabsorption Modulated Laser (EML): Set-up and Optimization* Technical Note, TN00-008OPTO.

In DWDM systems, the use of laser devices tuned to specific wavelengths places specific constraints on the wavelength stability of those devices, both as a function of time and environmental conditions, particularly temperature. The available wavelength space between the chosen channels will be apportioned among the various components in the system by the system designer. In particular, the optical MUX and deMUX components, to the extent that they require their own wavelength drift budget over temperature and life, can leave only a small region in which the laser wavelength can drift or age before an overall system end-of-life condition is reached.

Agere has extensively characterized wavelength stability over temperature and over life for a variety of source products. The EML device has been particularly well characterized and the results presented here are intended to assist the system designer in incorporating the EML into leading-edge DWDM designs.

Contributions to Wavelength Change (Drift) of EML Sources

This document examines six critical aspects of device and system performance that need to be considered when establishing the budget for changes in wavelength for a component or system, including:

- Change in wavelength with case temperature variation (λ vs. T_{CASE})
- Change in wavelength with CW drive current to the DFB section (λ vs. I_{DFB})
- Change in wavelength owing to short-term changes in the EML chip temperature (λ vs. T_{CHIP})
- Aging of the thermistor
- Change in wavelength under environmental stress conditions
- Wavelength aging of the EML module

Change in Wavelength with Case Temperature Variation (λ vs. T_{CASE})

Although EML devices are temperature controlled by a thermoelectric cooler, all cooled optical sources are subject to some change in wavelength as the ambient or case temperature is varied. In particular, thermal crosstalk between the EML chip and the thermistor, and other aspects of the thermal design of the package, contribute to the overall stability performance. Figure 1 shows the typical wavelength vs. case temperature performance of the EML, using twelve devices chosen at random.

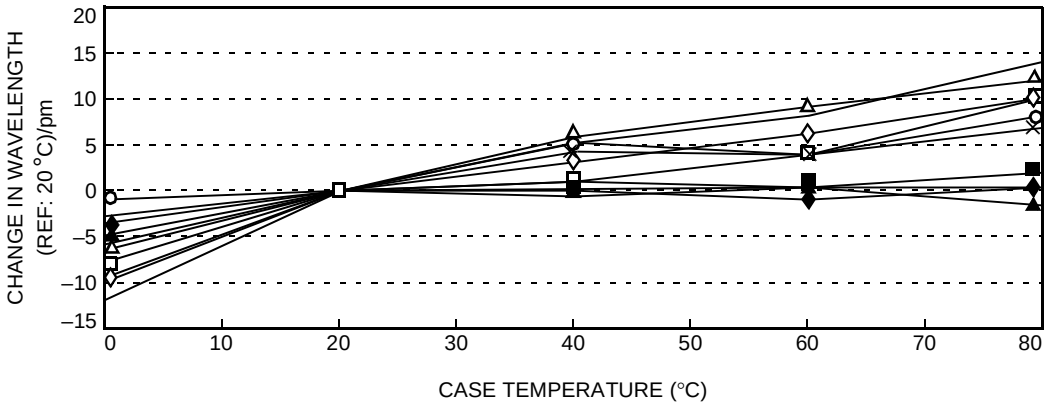

Figure 1. EML Wavelength vs. Case Temperature (2.5 Gbits/s and 10 Gbits/s EML)

1-1110(F)

From these and other results, a worst-case change in case temperature of ±15 pm is guaranteed for the operating case temperature range 0 °C to 70 °C.

Change in Wavelength with CW Drive Current to the DFB Section (λ vs. I_{DFB})

Due to the increased thermal load in the CW section as the drive current is increased, a small, corresponding increase in wavelength is observed. Figure 2 presents data showing typical wavelength vs. DFB current and indicates a worst-case value $d\lambda/dI_{DFB}$ of <0.007 nm/mA, or <7 pm/mA.

In a system using constant power control, the increase in CW drive current over the life of that system should be taken into account, and the worst-case coefficient quoted above may be used to calculate the corresponding change in wavelength that is expected. This data can also be used to predict the wavelength shift associated with any short-term changes in the DFB current, which the designer of the automatic power control (APC) circuit can predict.

Note: The wavelength-aging predictions discussed in the section on Wavelength Aging of the EML Module, page 7, include an allowance for the increase in CW drive current over life, which is described above. Therefore, there is no need to include any allowance in cases where a reliability forecast based on the results of wavelength aging of the EML module is used.

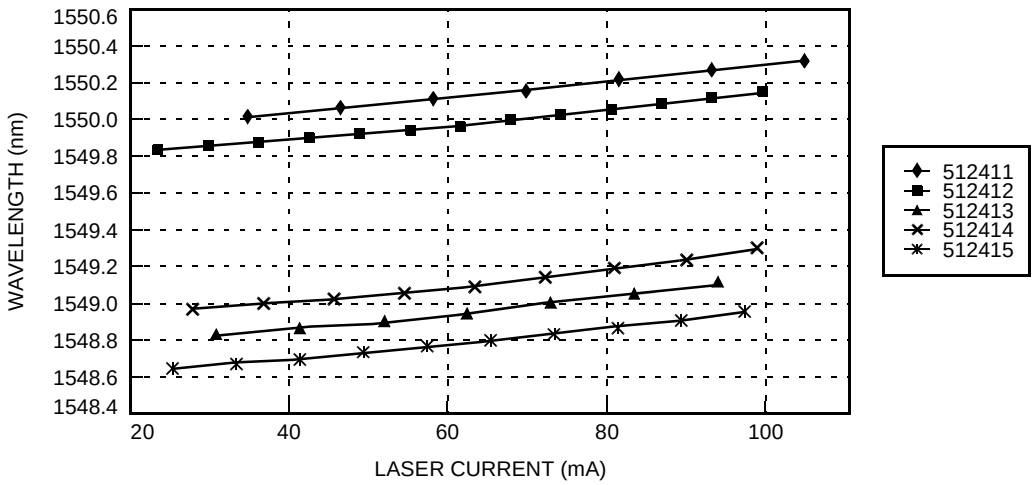

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Figure 2. Change in Wavelength with CW Drive Current

Change in Wavelength Owing to Short-Term Changes in EML Chip Temperature (λ vs. T_{CHIP})

This is an additional contribution to the change in temperature of the EML chip, and depends on the integrity of the feedback loop that controls the thermoelectric cooler (TEC). Most TEC control loops are capable of controlling the chip temperature to one- or two-tenths of 1 °C. Once the system designer has identified any temperature variation owing to this cause, the data in Figure 3 may be used to identify the resulting change in wavelength.

The two curves shown in Figure 3 represent modulator bias conditions of 0 V, and a typical nominal modulator bias condition of pkg-avg.

The results indicate a median coefficient, $d\lambda/dT_{CHIP}$, of 0.85 A/°C, or 85 pm/°C, with a worst-case (+3 σ) value of 106 pm/°C.

Note: The wavelength-aging predictions, discussed in the section on Wavelength Aging of the EML Module, page 7, include an assumed value of ±0.25 °C for short-term changes in chip temperature. Therefore, there is no need to include any allowance for this reason where the results of the wavelength-aging simulation will be used, unless the predicted temperature change exceeds ±0.25 °C.

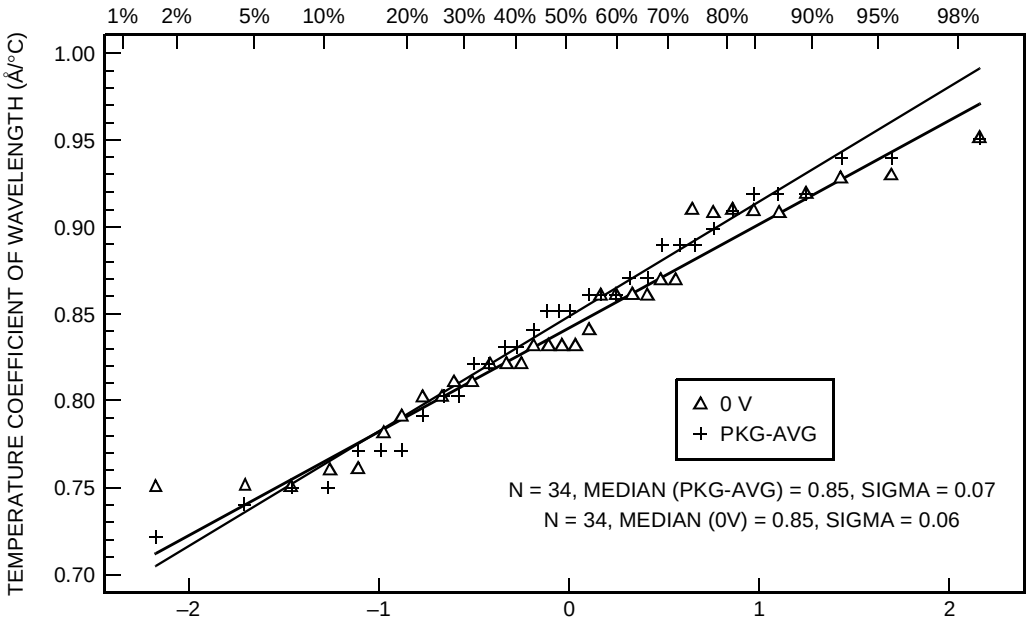

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Figure 3. Distribution of EML Wavelength vs. (Chip) Temperature

Aging of the Thermistor

Figure 4 presents data showing the measured aging of the thermistor resistance under stress conditions at 125 °C for 1000 hours. A median resistance change of 0.28% with a log normal dispersion of 1.0 is observed.

For most applications, therefore, the results indicate that thermistor aging is negligible in terms of overall device performance.

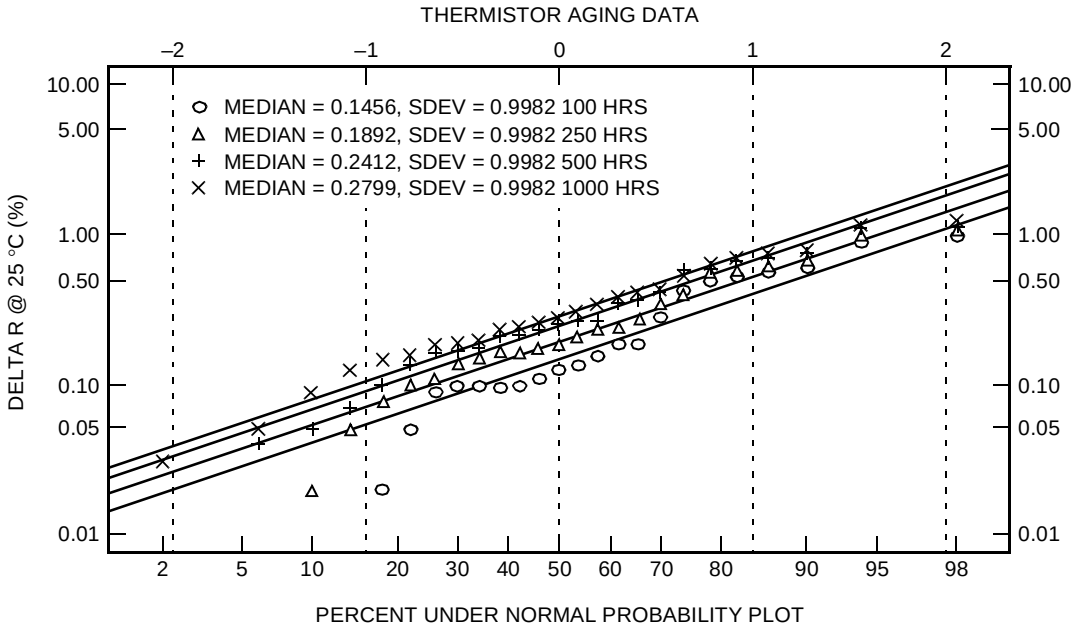

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Figure 4. Thermistor Accelerated Aging Under Stress Conditions

Change in Wavelength Under Environmental Stress Conditions

The following findings, Figure 5a and Figure 5b, are the result of characterization of package performance, showing change in wavelength during temperature cycling and high-temperature soak at an ambient temperature of 85 °C. They are provided for information only, to indicate wavelength stability performance under worst-case qualification stress conditions. Since normal operation will take place in a far more stable environment, where temperatures are typically <85 °C and the package is not subject to extreme stress conditions, it is not necessary to factor the changes shown below into the overall operating wavelength budget for most applications.

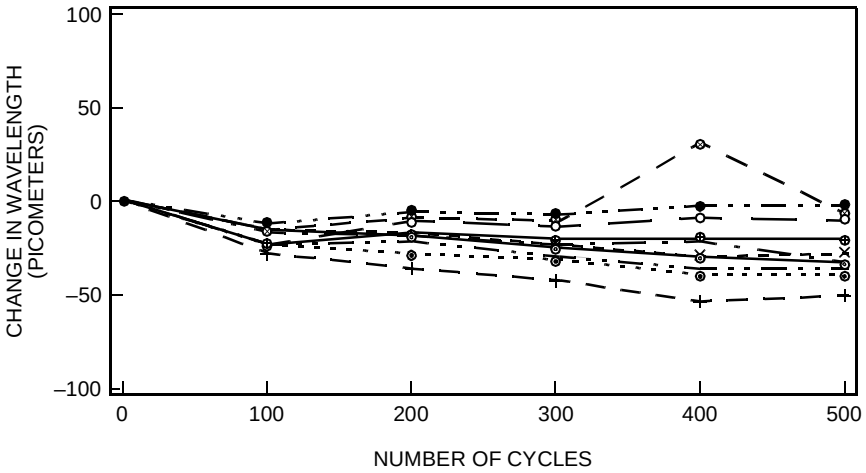

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Figure 5a. Change in Wavelength During –40 °C to +85 °C Temperature Cycling

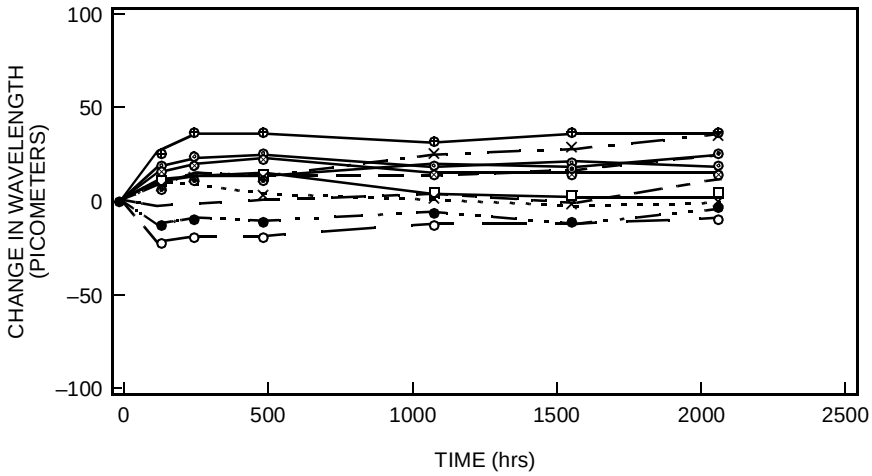

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Figure 5b. Change in Wavelength During High-Temperature (85 °C) Bake

Wavelength Aging of the EML Module

Agere has extensively characterized the wavelength-aging performance of the EML and other laser devices. The magnitude and mechanisms of wavelength aging are very well understood. In the case of the EML, all aging of the modulation section is found to be negligible, and the CW (DFB) section effectively contributes all the efficiency and wavelength change over life. The wavelength aging is thus similar in nature and magnitude to that observed on Ageres' stand-alone CW and direct-modulated DFB lasers, since the chip structures are similar. In both cases, the total aging is extremely low, such that the changes are not easy to measure accurately.

The procedure used to measure wavelength aging involves a test of the entire EML package under stress conditions at a case temperature of 100 °C and a CW drive current of 200 mA, with a bias voltage to the modulator of –3 V. Figure 6a shows an example of four (from a total of 200) devices, during testing to 600 hours under these conditions.

All devices tested show the same behavior. These results and additional characterization isolate two observable aging mechanisms. One is due to an initial, nonbias-activated transient, the other is the result of a long-term, repeatable, small bias-activated aging.

Nonbias-Activated Transient

An initial, nonbias-activated transient, resulting in a shift to the red, or higher wavelengths is due to packaging effects, in particular the relaxation of stresses induced during bonding of the EML chip to its substrate.

Further experiments have revealed that at normal operating temperatures (<100 °C), not only the rate but also the magnitude of the nonbias-activated transient is significantly smaller than is shown under stress conditions in Figure 6a.

The raw data on 200 devices, from which the data on four devices shown in Figure 6a was extracted, suggests a median magnitude of the nonbias-activated transient of ~30 pm under stress conditions. Aging measurements performed at lower temperatures indicate that under normal operating conditions of about 25 °C, the actual median value (μ) is ~15 pm, described by a lognormal distribution with σ = 0.4.

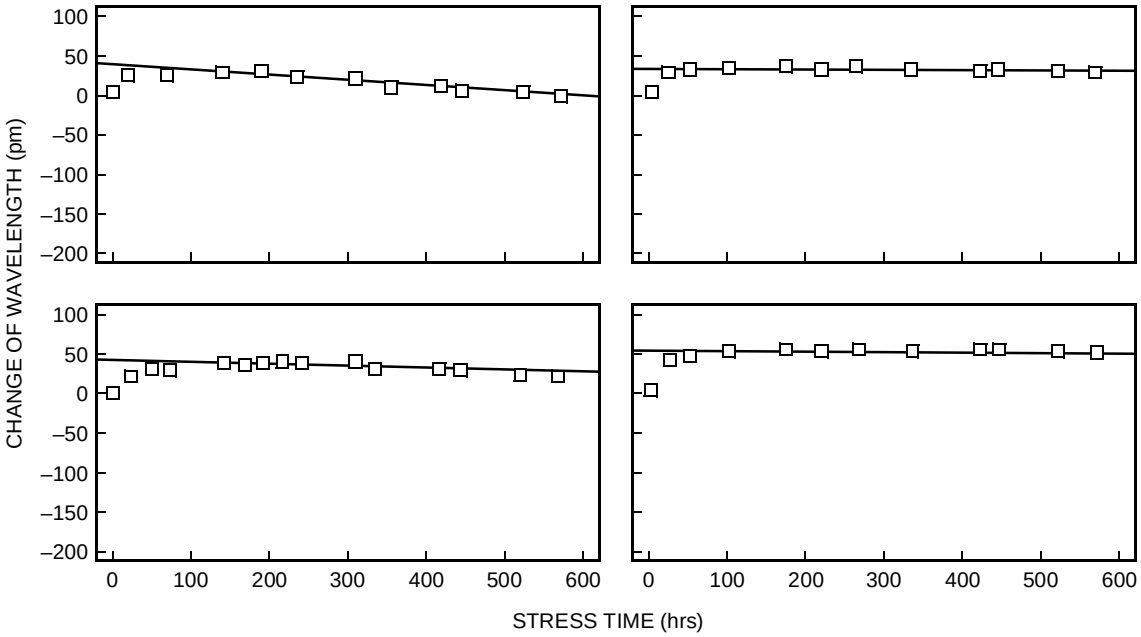

Figure 6a. Example of Typical (Stressed) EML Wavelength-Aging Characteristics

Wavelength Aging of the EML Module

(continued)

Long-Term, Bias-Activated Aging

Long-term, repeatable, and small bias-activated aging to the blue, or lower, wavelengths is a result of the decrease in effective refractive index that occurs as the free carrier concentration increases over life, and is consistent with the classical DFB device aging mechanism.

Note that Figure 6a shows aging under conditions of constant current. When operating under constant power, as described on page 3, the effect of increasing drive current over life (required to maintain constant output power from the EML as the CW section ages over life) adds an additional, very small shift to the longer wavelengths (red), which opposes the blue shift observed. The simulation that follows accounts for this change and so the results presented are representative of conditions of constant power rather than constant current.

Simulated Analysis

The distribution of observed changes for mechanisms described here has been characterized separately and in combination. An activation energy (0.68 eV) has been calculated from the available data, and a simulation performed using a Monte Carlo analysis, which predicts the total wavelength shift under constant power over 15 years of operation, at a nominal temperature of 25 °C.

Items included in the simulation are the following:

- The nonbias-activated red transient and long-term blue aging.
- The nonbias-activated transient is described by the lognormal distribution referred to in the preceding section with $\mu = 15$ pm, $\sigma = 0.4$.
- Ohmic heating due to bias current increase over life, for constant power operation.
- Short-term wavelength drifts due to chip temperature variations, modelled by a uniform distribution in temperature variations of ±0.25 °C, as described in the section on Change in Wavelength Owing to Short-Term Changes in EML Chip Temperature, page 3.

Not included in the simulation is any allowance for wavelength variation with case temperature ($d\lambda/dT_{CASE}$), for which an additional allowance of up to ±15 pm should be made, as described in the section, Change in Wavelength with Case Temperature Variation, page 2. It is left to the system designer to determine the allowance to be made for this factor, since the actual temperature profile can vary substantially from system to system, depending on the individual application.

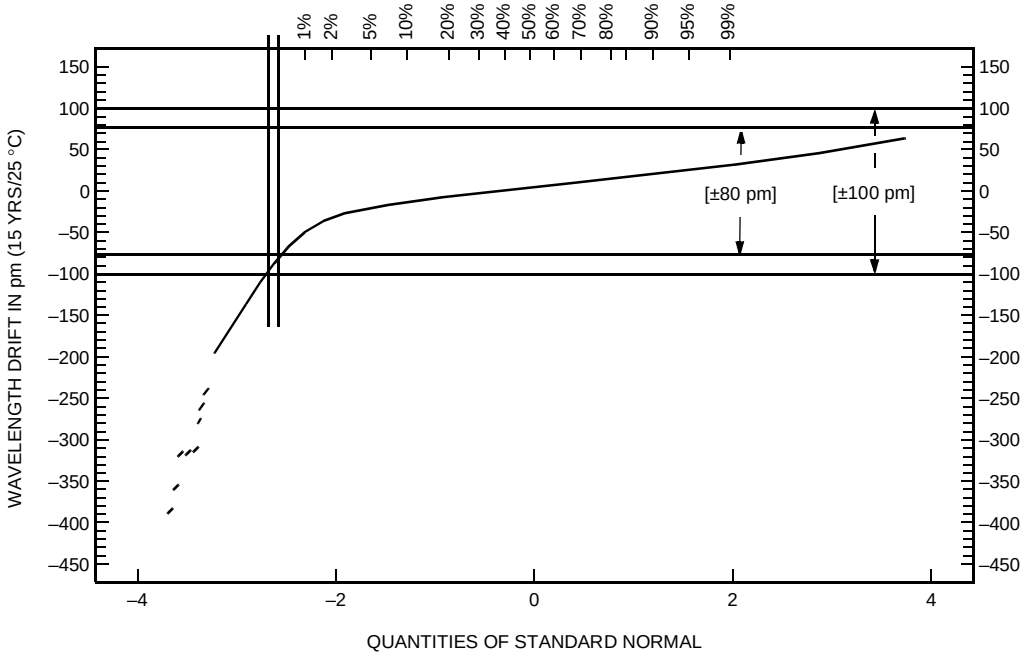

Figure 6b. Simulated Wavelength Shift of EML at 25 °C, Constant Power, Over 15 Yrs.

Wavelength Aging of the EML Module

(continued)

Simulated Analysis (continued)

Also shown is some arbitrary criteria for a system employing 100 GHz ITU channel spacing, where an allowable wavelength shift of ±100 pm and ±80 pm total are assumed. In fact, the allowable shift before an end-of-life condition is reached will vary from system to system, according to the factors discussed elsewhere in this document. The values shown are chosen, from experience, as an example that could represent a typical system.

Using these values, it is concluded that the allowed aging will support operation in a system where the allowable wavelength aging is ±80 pm or greater, with an extremely low (<200 FIT) hazard rate. In most cases, this will support systems employing 100 GHz channel spacing with no issue. For systems at 50 GHz spacing, the use of a wavelength locker is advised, and the reader is referred to Ageres' range of EML-based transmitter products, which employ wavelength tunable sources and integrated wavelength lockers (e.g., the C488-Type and C489-Type transmitters).

Summary and Conclusion

Table 1. Summary of Key Coefficients and Stability Performance

Parameter	Value/Comments
1. Wavelength Variation with Case Temperature	±15 pm max is assured from 0 to 70 °C.
2. Wavelength Variation with DFB Current	<7 pm/mA is assured.
3. Wavelength Variation with Chip Temperature	85 ± 21 pm/°C is assured.
4. Thermistor Aging	≤0.3% is predicted (i.e., negligible).
5. Wavelength Variation Under Environmental Stress Conditions	Refer to page 6.
6. Wavelength Aging of the EML Module	±80 pm total aging is supported (prediction includes contributions from Table items 2, 3, and 4).

The user should now be in a position to identify and quantify the key contributors to wavelength change in a typical DWDM system, and to understand and predict the performance of Ageres' E2500 series EML component in that system. It should be possible to predict the need for external locking elements or changes in the design to accommodate the required wavelength drift budget.

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August 2000
TN00-012OPTO

agere systems

Technical Note
May 2000

Electroabsorptive Modulated Laser (EML): Setup and Optimization

Introduction

The Agere Systems Inc. E2500 series Electroabsorptive Modulated Isolated Laser Module (EM-ILM or EML) combines an integrated modulator and CW laser in a single semiconductor chip, providing a compact and cost-effective solution for extended-reach transmission up to and beyond 600 km at 2.5 Gbits/s. Products for
10 Gbits/s operation, including a version with an integral driver IC, are also available.

In most applications, the EML can replace external optical modulators, such as $LiNbO_3$ Mach-Zender-type devices, and offers space-saving, economy, and ease-of-use among its advantages. The information offered here is intended to acquaint the user with the primary features and characteristics of the EML device as well as the steps required to optimize its performance in long-reach systems.

Operating at 1.5 µm wavelength, and offering discrete wavelengths in the 1.5 µm region selected to the ITU-T grid, the EML chip is supplied in an ultrastable, industry-standard package, with thermoelectric cooler and optical isolation.

The module meets the intent of the Bellcore TA-TSY-000468 qualification standard, and is extremely reliable, offering a median lifetime of approximately 50 years under typical operating conditions.

To ensure that sufficient optical power reaches the receiver, the EML is typically coupled with several erbium-doped fiber amplifiers (EDFAs), such as Agere's 1724-Type. The standard 2.5 Gbits/s EML product is specified for use up to 360 km (E2505-Type) and 600 km (E2502-Type). Agere's 10 Gbits/s EML product is available as E2560-Type (40 km, without integral driver IC) and E2580-Type (40 km, with integral driver IC). Longer span lengths at 10 Gbits/s are also addressed with E2561-Type (60 km, without IC) and E2581-Type (80 km, with IC).

Other related products are Agere's LG1626DXC modulator driver for operation at 2.5 Gbits/s, and a range of PIN- and APD-based receiver products for high-speed applications at 2.5 Gbits/s and 10 Gbits/s.

Typical Performance

The key feature that distinguishes the EML from directly modulated laser devices is its extremely low chirp. The chirp, or variation in wavelength during a sequence of optical bits, is typically less than 0.02 nm, or 0.2 Å, from peak to peak (zero to one) for 2.5 Gbits/s, 360 km devices, and even lower for devices used at >600 km. This enables transmission over extremely long distances in optical fiber with a minimum amount of chromatic dispersion.

Figure 1 shows an example of an E2502-Type device operating with low dispersion penalty in a system application at 2.5 Gbits/s and up to distances greater than 1000 km. Note that at 328 km, the dispersion penalty is negative. This is an intentional feature that is discussed in detail in the following information.

The emitted wavelength of the device increases with increasing chip temperature with a median coefficient, $d\lambda/dT$, of 0.085 nm/°C. Each delivered device is accompanied by a record of the thermistor resistance for the set-temperature that corresponds to the specific ITU wavelength.

For an in-depth description of the typical performance of the EML over temperature in dense wavelength-division multiplexing (DWDM) systems, and its typical wavelength aging characteristics, please refer to the *Use of Electroabsorptive Modulated Laser Devices in Dense WDM Applications* Technical Note (TN00-012OPTO).

Also documented with each device is a value for the forward current in the distributed-feedback (DFB) section, in which the rated power is achieved. If the rated power is achieved at a forward current of 50 mA or less, then 50 mA is the value used for the other parameter testing. Operating the DFB section at a forward current of less than 50 mA, or greater than 100 mA, is not recommended. The reason for the minimum limit is that the relaxation oscillation frequency of the device at < 50 mA will be reduced into a region where the chirp performance of the device will be adversely affected.

In general, the chirp improves with increasing DFB current. The noise performance (RIN) also improves and, of course, the power output of the device increases. The extinction ratio degrades slowly with increasing DFB current.

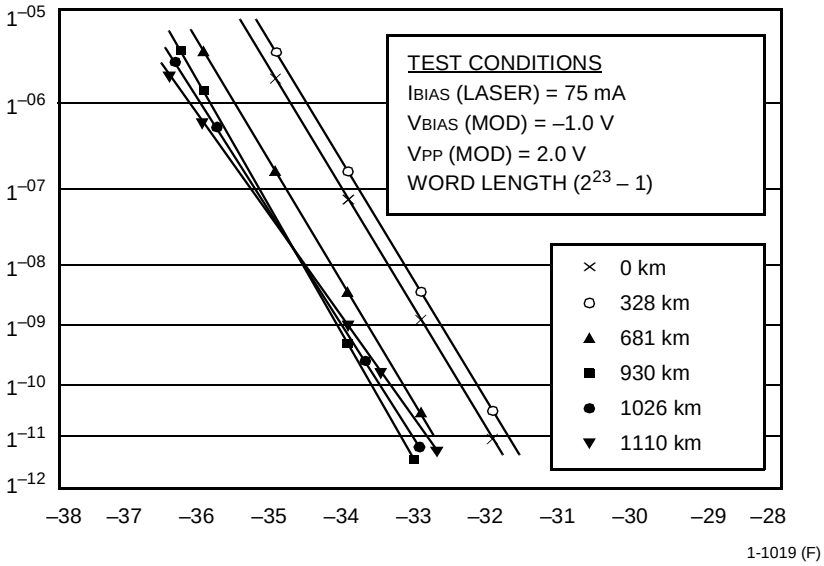

Figure 1. Example of an EML in System Performance

Setup and Tuning

1. Using the value provided for the thermistor resistance, and with the DFB current set at 75 mA, and zero bias voltage applied to the modulator, measure and record the wavelength and optical power.
2. Referring to Figure 2 if necessary, adjust the voltages applied to the modulation section to the values shown in Table 1.
3. Adjust V_{ON} (with Vp-p constant) by up to 0.2 V from the values stated above, as a coarse power control. Adjust the DFB current as a fine power control, and fine-tune the wavelength by adjusting the operating temperature if required.
4. Adjust the eye crossover to between 30% and 50% of the optical power, where allowed by the EA driver.

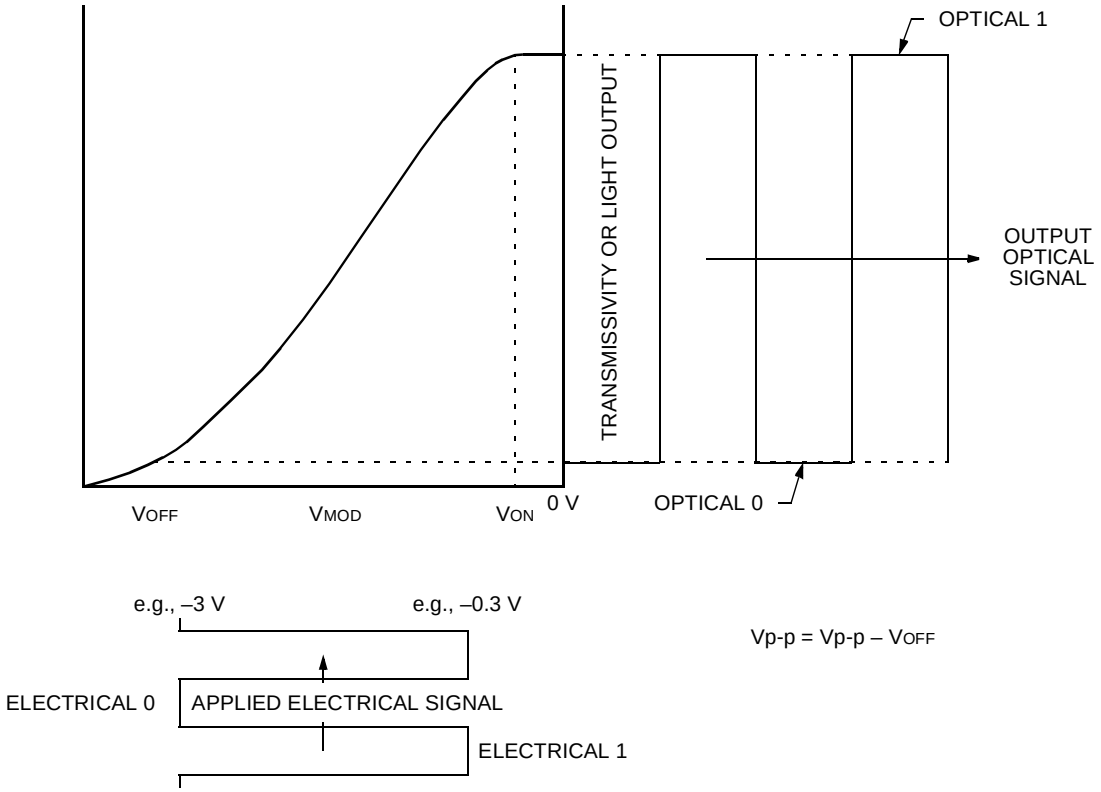

Figure 2. Light Versus Applied Voltage (Transfer) Characteristic of the Modulator

Table 1. On-State and Peak Voltage Adjustments for EMLs.

Pin Number	On-State (one) Voltage (V_{ON})	Peak-to-Peak Voltage (Vp-p)
600 km @ 2.5 Gbits/s/E2502xx	–0.3 V	2.0 V*
360 km @ 2.5 Gbits/s/E2505xx	–0.3 V	2.0 V*
10 Gbits/s/ E256xx or E258xx	–0.5 V	2.0 V†

* Or higher, as required to achieve the minimum desired extinction ratio.

† For the 10 Gbits/s version with integral driver IC, refer also to the *E2580 EML with Integral Driver IC: Pin Definitions and Operation* Application Note (AP00-023OPTO).

Further Optimization: Chirp, Pulse Clipping, and Linear Pulse Compression

Further improvements in performance can be achieved by optimizing the applied voltage to the modulator for the specific application. As may be seen in Figure 2, reducing the on-state voltage (i.e., the voltage level corresponding to the electrical one), while typically offering the benefit of reducing the dispersion penalty, also reduces the output power. The optimum trade-off between the two will depend on the system design. For example, in a system where the EML is followed immediately by a booster EDFA, power is not at a premium, and system dispersion can be further improved by reducing the on-state voltage from the values shown in Table 1. Operating the modulator with a positive on-state voltage is not recommended because it adversely affects the dispersion performance.

A specific safeguard is recommended with respect to the on-state voltage. The EML is subject to a self-biasing (photocurrent) mechanism, which means that if the on-state voltage is not controlled, particularly if the dc component of the modulator drive is left floating, the value of the on-state voltage can inadvertently be allowed to become positive. It is important that this is avoided, preferably using a control circuit as shown in Appendix A.

To make further adjustments in the available parameter space, it is necessary to understand some additional characteristics of the Agere EML design.

Figures 3A—3D show four modulation scenarios for the EML modulator. In each case, an electrical signal is applied to the X axis (modulation voltage) and an optical signal is produced on the Y axis (light output), as introduced in Figure 2.

Figure 3A describes an ideal situation in which the applied electrical signal from the driver is perfect, i.e., it contains no noise or distortion components. The on-state voltage is zero, representing a nominal chirp value, and the electrical signal is translated into a perfect optical signal.

Figure 3B represents a more realistic example in which the incoming electrical signal from the driver is imperfect, and the on-state voltage has been reduced from 0 V to some negative value in order to reduce chirp. The output optical signal faithfully reproduces the incoming electrical signal, including all noise and distortion elements. Note in particular that the on-state bias voltage corresponds to a part of the characteristic in which the slope (dL/dV) is high, meaning that noise elements in the electrical one are accurately reproduced optically. In this example, the EML is satisfying its minimum performance requirement.

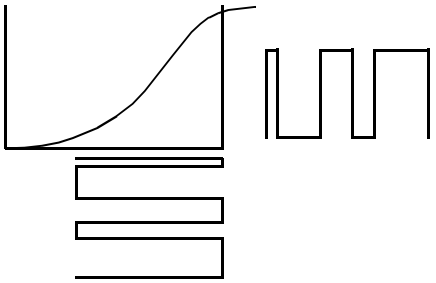

Figure 3A. EML with Perfect Applied Electrical Signal

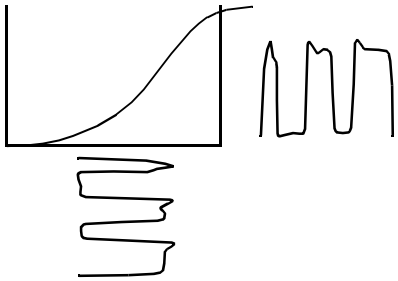

Figure 3B. EML with Imperfect Applied Electrical Signal

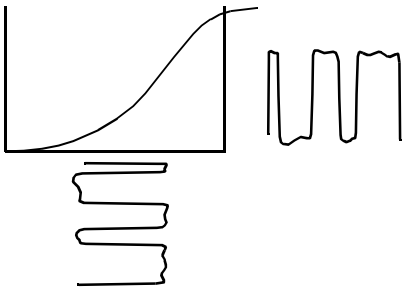

Figure 3C. EML with Optimized Impedance

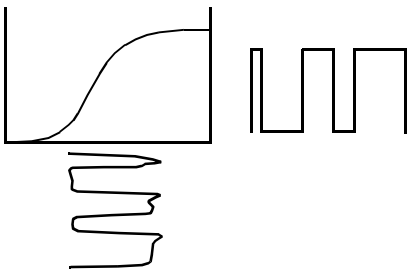

Figure 3D. EML with Modified Transfer Characteristics

1-1017 (F)

Figure 3. Chirp, Impedance Matching, and Modulator Design in the EML

Further Optimization: Chirp, Pulse Clipping and Linear Pulse Compression

(continued)

Figure 3C shows the result of optimization of the impedance in the EML package. Optimization is straightforward to ensure that the device behaves as a 50 ¾ impedance in the on and off states. However, the impedance of the modulation section in any EML design will fall significantly during the transition from an electrical one to an electrical zero, or vice versa. This can present problems when interfacing to a driver that is designed to assume a 50 ¾ load at all times, and can be partially or wholly responsible for a poor electrical input signal, such as that shown in Figure 3B.

In the E2500-Type EML package, the problem is addressed by using an optimized combination of capacitance and induction, which ensures the effective impedance remains as close as possible to 50 ¾ throughout the transition between states.

Figure 3D shows an additional design feature of the current design that will be used further in future design iterations of the modulator. Since the on-state voltage for long-reach applications can be reduced to control the chirp, the one state can occur in a region of the transfer characteristic where the slope (dL/dV) is high, as outlined in the discussion of Figure 3B.

By modifying the shape of the transfer characteristic as shown, the one state for reduced chirp will correspond to an area of greatly reduced dL/dV, with the result that noise or distortion components on the optical one state will be clipped or suppressed. This clipping feature can minimize the effect of an imperfect incoming electrical signal.

Therefore, and to review, in making further adjustments to those described in the Setup and Tuning Proposal section, it should be noted that:

- The trade-off between chirp and output power can be optimized by adjusting on-state bias voltage while maintaining a constant peak-to-peak modulation voltage. Increasing DFB current can improve both chirp and RIN, at the expense of extinction ratio.
- When reducing the on-state bias voltage in order to reduce chirp, care should be taken to examine the incoming electrical signal, since this action will also reduce the inherent clipping effect of the modulator.

Referring back to the results presented in Figure 1, the reason why adjusting on-state bias voltage can result not only in reduced dispersion penalty but in negative dispersion penalty as well can be explained by referring to Figure 4 below.

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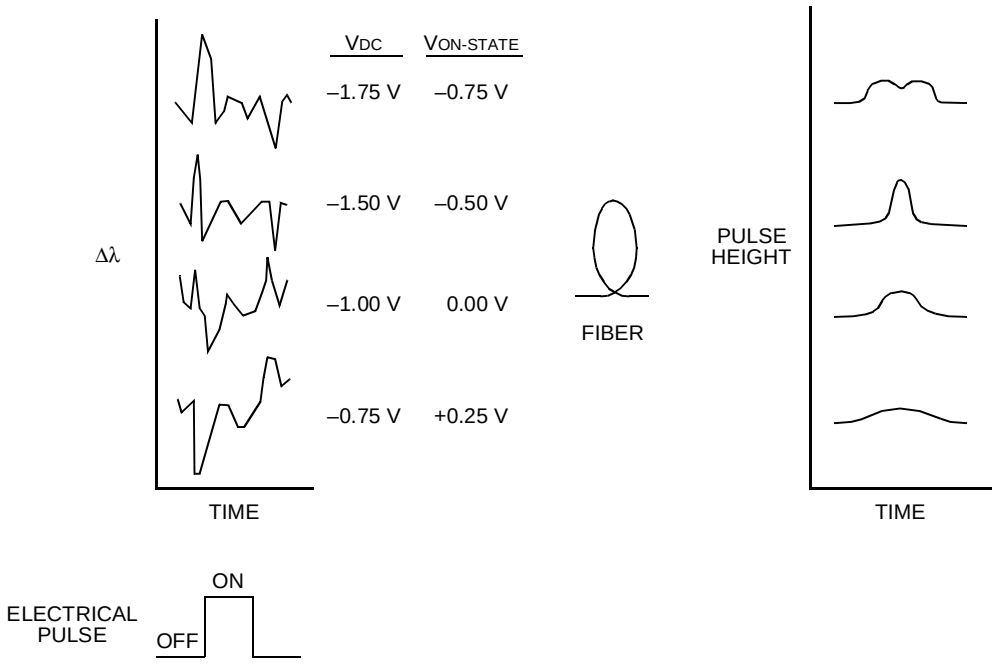


1-1016 (F)

Figure 4. Linear Pulse Compression

Further Optimization: Chirp, Pulse Clipping and Linear Pulse Compression (continued)

The results presented on the first graph show chirp, $\lambda\Delta$, as a function of time during the applied electrical pulse. They are actual measurements of the E2500-Type device. As the on-state is varied while the midpoint modulation voltage, Vdc, is adjusted in order to maintain a constant peak-to-peak modulation voltage of 2 V, the chirp of the leading edge of the pulse changes relative to the trailing edge of the pulse.

Consider the cases at $V_{ON\text{-}STATE}$ = 0 V and –0.5 V. In the first case, the net chirp at the leading edge of the pulse is negative, or blue, compared to the chirp at the trailing edge. Therefore, the leading edge of the pulse will travel more quickly in the optical fiber because light at lower wavelengths (higher frequencies) travels more quickly in standard fiber than light at higher wavelengths. The pulse, therefore, will broaden in time as it travels along the fiber, and the net result will be a positive dispersion penalty.

In the second case, at $V_{ON\text{-}STATE}$ = –0.5 V, the converse happens. The net chirp at the leading edge becomes positive with respect to the trailing edge, the leading edge travels more slowly in fiber than the trailing edge, and the pulse is compressed as it travels through the fiber. The net result is a negative dispersion penalty.

The examples at $V_{ON\text{-}STATE}$ = –0.75 V and +0.25 V show what occurs at the extremes of each case. At –0.75 V, the negative chirp becomes so pronounced that the leading edge of the pulse is overtaken by the trailing edge. The optical pulse collapses in the fiber and the dispersion penalty again becomes positive. At +0.25 V, extreme positive chirp at the trailing edge simply leads to excessive pulse broadening, and the resulting dispersion penalty in the system is high.

Figure 5 offers a practical demonstration of the effect described above, in a simple system simulation.

In this example, a device chosen at random is used to transmit a pseudorandom bit sequence in 300 km of fiber, using several EDFAs and Agere's standard 2.5 Gbits/s receiver (1319-Type), limiting amplifier, and clock and data recovery. An optical filter is used at the receiver.

As the on-state bias, V_{ON}, is varied, it can be seen that through linear pulse compression, the dispersion penalty goes from ~2 dB at 0 V to a negative value at –0.3 V. As V_{ON} is reduced further, the dispersion penalty again becomes positive.

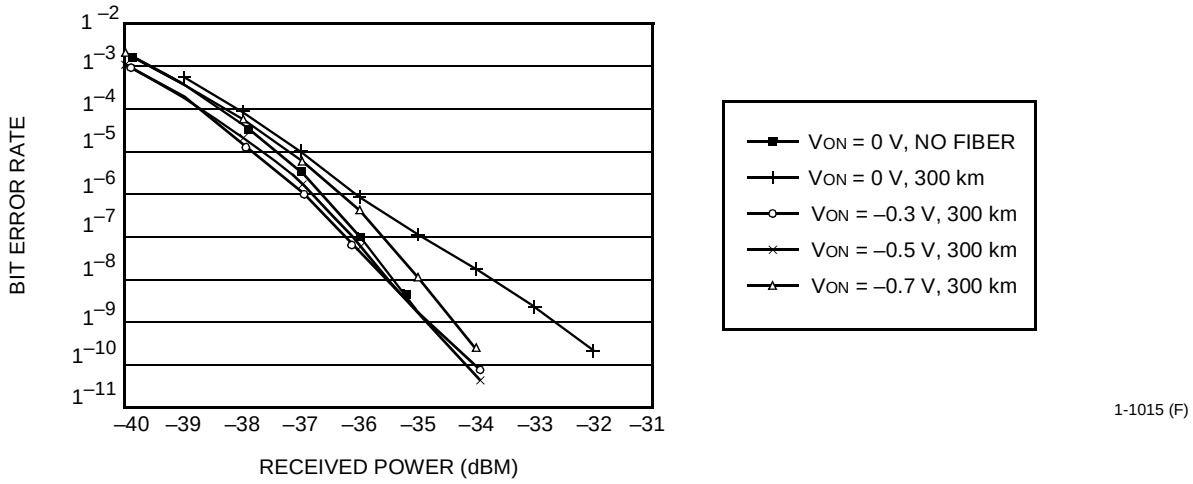


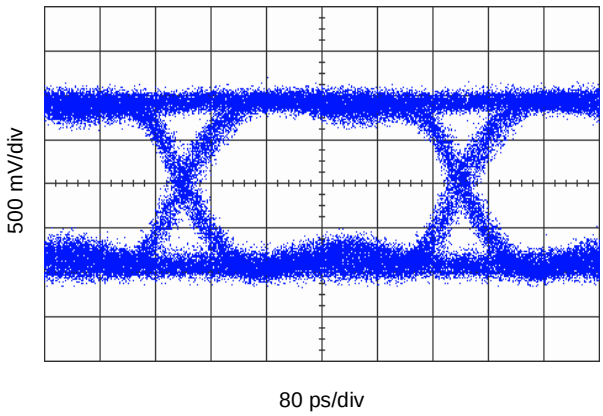
Figure 5. Dispersion Penalty Versus Modulator On-State Voltage for the E2505xx EML

Conclusion

The user should now be equipped to optimize the performance of the EML in a variety of digital system applications. By adjusting the bias and modulation voltages as recommended, optical linear pulse compression and dispersion, pulse clipping, optical output power, and extinction ratio can all be controlled. Additional adjustments in chirp, RIN, and extinction ratio can be achieved by optimizing the DFB current.

For further information on the use of EMLs in DWDM systems, and in particular, for details of device performance over case and chip temperature ranges, and typical wavelength aging performance over life, refer to the forthcoming *Use of Electroabsorptive Modulated Laser Devices in Dense WDM Applications* Technical Note.

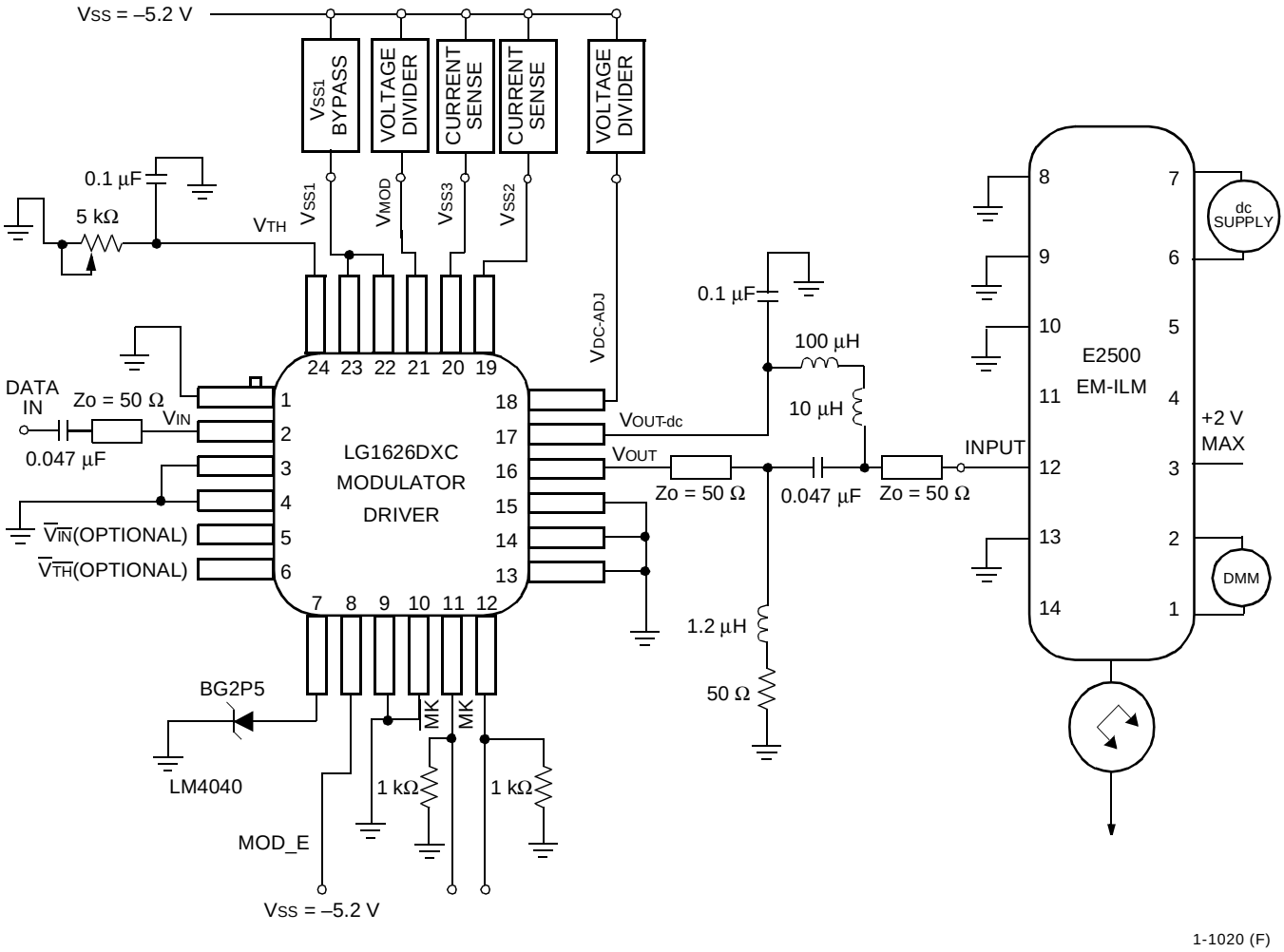
Appendix A



1-1015 (F)

Figure 6. Typical Optical Eye Diagram

Appendix A (continued)



1-1020 (F)

Figure 7. Typical Optical Evaluation of the LG1626DXC and E2500-Type EM-ILM*

* Suggested inductors:
Coilcraft †, 1.2 µH, part No.1008LS-122XKBC; 10 µH, part No. 1008LS-103XKBC; 100 µH, part No. 90-37.
National Semiconductor ‡, bandgap reference LM4040.

† *Coilcraft* is a registered trademark of Coilcraft Inc.

‡ *National Semiconductor* is a registered trademark of National Semiconductor Corp.

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1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
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JAPAN: **(81) 3-5421-1600** (Tokyo), KOREA: **(82) 2-767-1850** (Seoul), SINGAPORE: **(65) 778-8833**, TAIWAN: **(886) 2-2725-5858** (Taipei)
EUROPE: **Tel. (44) 7000 624624**, FAX (44) 1344 488 045

LTC1923

High Efficiency Thermoelectric Cooler Controller

July 2001

FEATURES

- **High Efficiency, Low Noise Topology**
- **Adjustable Output Slew Rate Reduces EMI**
- **Full-Bridge Controller for Bidirectional Current Control**
- **Adjustable Pulse-by-Pulse Bidirectional TEC Current Limit**
- **Open/Shorted Thermistor Indication**
- TEC Voltage Clamping
- TEC Current, Voltage and Heat/Cool Status Outputs
- Low Current Shutdown: I_Q = 10µA
- Adjustable/Synchronizable Oscillator Frequency Reduces Filter Component Size and System Noise
- 2.5V Reference Voltage Output

APPLICATIONS

- Laser-Based Fiber Optic Links
- Medical Instruments
- CPU Temperature Regulators

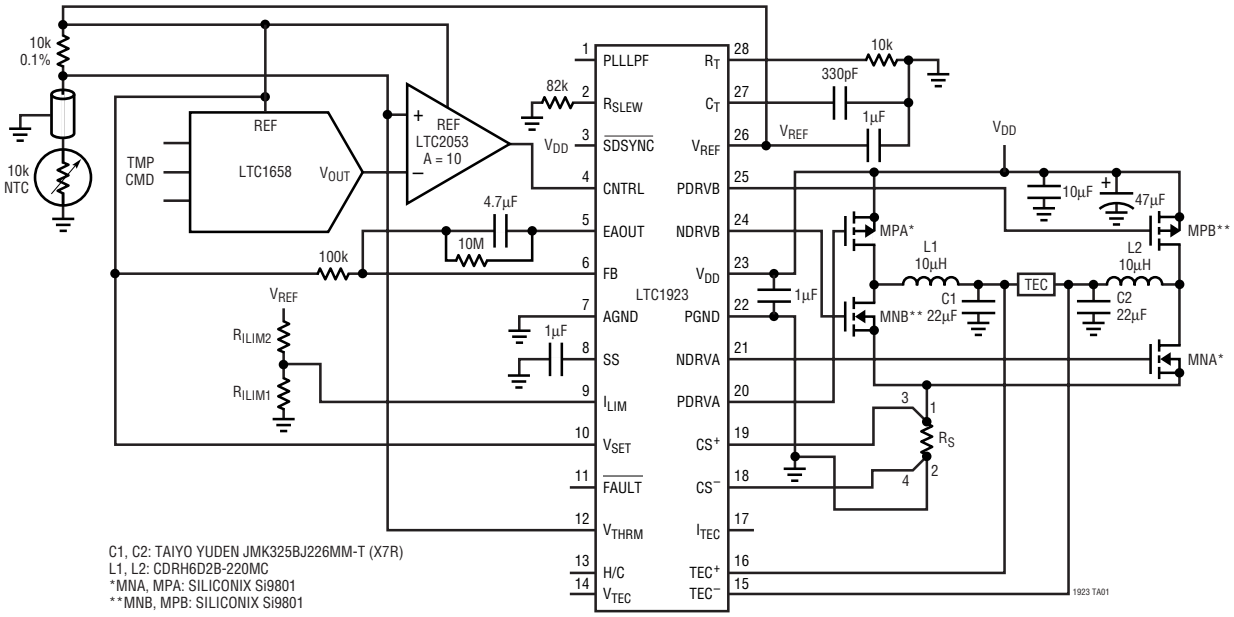
DESCRIPTION

The LTC®1923 is a pulse width modulator intended for thermoelectric cooler (TEC) or heater applications requiring either unidirectional or bidirectional drive circuits. All of the necessary control circuitry and two sets of complementary output drivers are integrated into the LTC1923 to drive a full bridge, providing an efficient means of bidirectional current flow to the TEC. An accurate temperature control loop to stabilize the temperature of a laser diode system is easily achieved with the addition of just a few external components. Typical temperature setpoint accuracy of 0.1°C is achievable with the LTC1923. Adding an instrumentation amplifier front end allows setpoint stability approaching 0.01°C.

The part features independent adjustable heating and cooling pulse-by-pulse current limit, current soft-start for controlled start-up, output slew rate control to reduce system noise, differential current sense and voltage amplifiers and a host of auxiliary circuits to protect the laser and provide redundant system monitoring. The LTC1923 is available in a 28-lead narrow SSOP package.

TYPICAL APPLICATION

Laser Temperature Control Loop Achieving Setpoint Stability Approaching 0.01°C



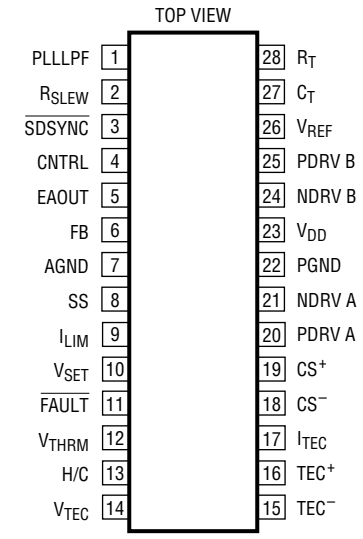
C1, C2: TAIYO YUDEN JMK325BJ226MM-T (X7R)
L1, L2: CDRH6D2B-220MC
*MNA, MPA: SILICONIX Si9801
**MNB, MPB: SILICONIX Si9801

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{DD} to GND ..... –0.3V to 6V
SDSYNC, R_{SLEW} ..... –0.3V to 6V
FB, CNTRL, V_{THRM}, I_{LIM} ..... –0.3V to 6V
CS^+, CS^-, TEC^+, TEC^- ..... –0.3V to 6V
FAULT, H/C ..... –0.3V to 6V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC1923EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, SDSYNC = V_{DD}, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
UVLO	Undervoltage Lockout	Low to High Threshold	●		2.6	2.7	V
UVHYST	Hysteresis	High to Low	●	50	130		mV
I_{DD}	Operating Supply Current	No Output Load, Outputs Not Switching			2	4	mA
I_{DDSHDN}	Shutdown I_{DD}	SDSYNC = 0V			10	25	µA
SHDNTH	Shutdown Threshold	Measured at PDRVA, PDRVB		0.3	0.8	1.4	V
Reference							
V_{REF}	Reference Output Voltage	No Load	 ●	2.462 2.450	2.5	2.538 2.550	V V
V_{REFGD}	V_{REF} Good Threshold	V_{REF} Rising Threshold	●		2.25	2.45	V
LDREG	Load Regulation	I_{LOAD} = –1mA to –10mA			10	25	mV
LINEREG	Line Regulation	V_{DD} = 2.7V to 5.5V			5	20	mV
V_{REFISC}	Short-Circuit Current	V_{REF} = 0V		10	20		mA
Oscillator and Phase-Locked Loop							
f_{OSCI}	Initial Oscillator Frequency	R_T = 10k, C_T = 330pF		190	225	260	kHz
f_{OSC}	Frequency Variation	V_{DD} = 2.7V to 5V	●	165	225	270	kHz
OSCPK	C_T Ramp Peak			1.4	1.5	1.6	V
OSCVLY	C_T Ramp Valley			0.4	0.5	0.6	V
C_{TICH}	C_T Charge Current	C_T = 0.3V, R_T = 10k			–150		µA

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, $\overline{SDSYNC}$ = V_{DD}, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{TIDIS}	C_T Discharge Current	C_T = 1.8V, R_T = 10k			150		µA
PLLGAIN	Gain from PLLLPF to R_T			–1.1	–0.9	–0.7	V/V
I_{PLLLPF}	Phase Detector Output Current Sinking Sourcing	 $f_{SYNC} < f_{OSC}$ $f_{SYNC} > f_{OSC}$			 12 –12		 µA µA
MSTTH	Master Threshold On PLLLPF Pin	Measured at $\overline{SDSYNC}$ Pin		V_{DD} – 0.7	V_{DD} – 0.4		V
SDDLY	Shutdown Delay to Output			20	45		µs
Error Amplifier							
V_{OS}	Input Offset Voltage	EAOUT = 1V, V_{CM} = 2.5V		–18		18	mV
AOL	Open-Loop Gain	EAOUT = 0.45V to 1.55V, CNTRL = 2.5V			80		dB
V_{CM}	Common Mode Input Range	EAOUT = 1V		0.2		V_{DD} + 0.2	V
I_{IB}	FB and CNTRL Input Bias Currents	FB = CNTRL = 1.25		–100		100	nA
V_{OH}	Output High	I_{LOAD} = –100µA			1.65		V
V_{OL}	Output Low	I_{LOAD} = 100µA			0.3	0.45	V
I_{SOURCE}	Sourcing Current	EAOUT = 1V, FB = 1V, CNTRL = 2V			–1.5	–0.5	mA
I_{SINK}	Sinking Current	EAOUT = 1V, FB = 1V, CNTRL = 0V		1	2		mA
GBW	Gain-Bandwidth Product	f = 100kHz (Note 3)			2		MHz
Current Sense Amplifier							
ACS	Amplifier Gain				10		V/V
CSOFF	Amplifier Offset			–15	–2	10	mV
I_{TECH}	Output High Voltage	I_{LOAD} = –50µA		V_{DD} – 0.2	V_{DD} – 0.1		V
I_{TECL}	Output Low Voltage	I_{LOAD} = 50µA			0.1	0.2	V
f3dB	–3dB Frequency	(Note 3)			500		kHz
I_{LIMTH}	Current Limit Threshold	Measured at CS^+, CS^-	●	125	145	165	mV
I_{LIMDLY}	Current Limit Delay to Output				300	450	ns
SSI_{CHG}	Soft-Start Charge Current	SS = 0.75V		–2.5	–1.5	–0.5	µA
SSI_{LIM}	Soft-Start Current Limit Threshold	SS = 0.5V, Measured at CS^+, CS^-		50	70	90	mV
I_{LIM}	I_{LIM} Current Limit Threshold	I_{LIM} = 0.5V, Measured at CS^+, CS^-		50	70	90	mV
TEC Voltage Amplifier							
ATEC	Amplifier Gain			0.98	1	1.02	V/V
TECOFF	Amplifier Offset	Measured at V_{TEC}, V_{CM} = 2.5V			–7		mV
TECCMR	Common Mode Rejection	0.1V < V_{CM} < 4.9V			60		dB
V_{TECH}	Output High Voltage	I_{LOAD} = –50µA		4.7	4.9		V
V_{TECL}	Output Low Voltage	I_{LOAD} = 50µA			0.1	0.3	V
f3dB	–3dB Frequency	(Note 3)			1		MHz
Output Drivers							
OUTH	Output High Voltage	I_{OUT} = –100mA		4	4.5		V
OUTL	Output Low Voltage	I_{OUT} = 100mA			0.7	1.2	V
t_{RISE}	Output Rise Time	C_{LOAD} = 1nF			20		ns
t_{FALL}	Output Fall Time	C_{LOAD} = 1nF			20		ns
t_{rSLEW}	Output Rise Time	C_{LOAD} = 1nF, R_{SLEW} = 10k			20		ns
t_{fSLEW}	Output Fall Time	C_{LOAD} = 1nF, R_{SLEW} = 10k			20		ns
t_{rSLEW}	Output Rise Time	C_{LOAD} = 1nF, R_{SLEW} = 100k			90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, $\overline{SDSYNC}$ = 5V, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{fSLEW}	Output Slew Fall Time	C_{LOAD} = 1nF, R_{SLEW} = 100k			90		ns
SLEWVT	R_{SLEW} Disable Threshold				2.75		V
DLY	Output Dead Time	R_T = 10k			90		ns
Fault							
OPENTH	Open Thermistor Threshold	V_{SET} = 5V, Measured with Respect to V_{SET}			–350		mV
SHRTTH	Shorted Thermistor Threshold	V_{SET} = 5V, Measured with Respect to GND			0.975		V
FLTV	Fault Output Low Voltage	1mA Into $\overline{FAULT}$, During Fault			150	300	mV
Direction Comparator							
DIRH	Low-to-High Threshold	TEC^- = 2.5V, Measured with Respect to TEC^- Sensed When H/C Toggles Low			50		mV
DIRL	High-to-Low Threshold	TEC^- = 2.5V, Measured with Respect to TEC^- Sensed When H/C Toggles High			–50		mV
HCV	H/C Output Low Voltage	1mA Into Pin, TEC^+ = 2.7V, TEC^- = 2.5V			150	300	mV

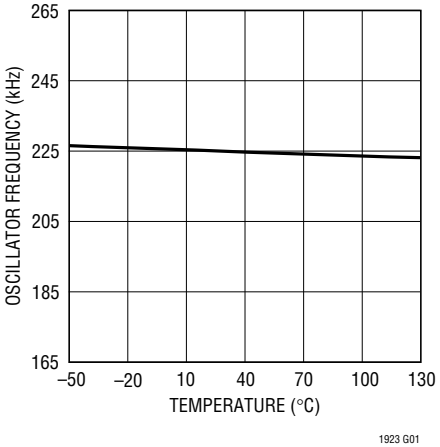
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1923E is guaranteed to meet specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

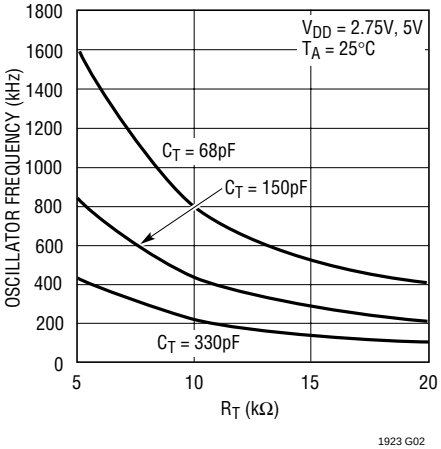
Note 3: Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

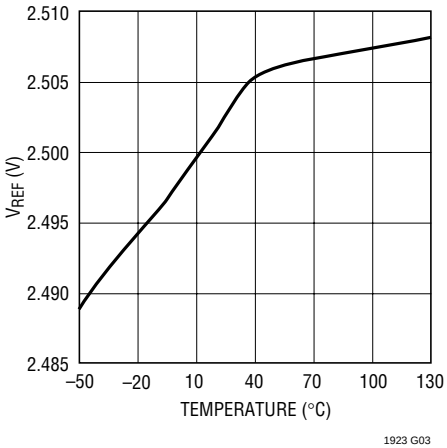
Oscillator Frequency vs Temperature



Oscillator Frequency vs R_T

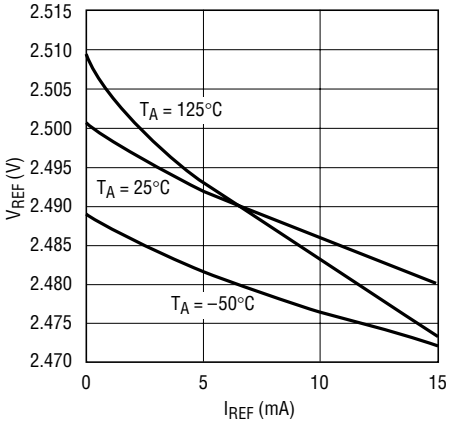


V_{REF} vs Temperature



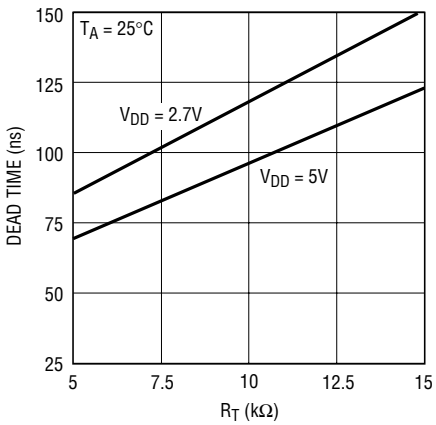
TYPICAL PERFORMANCE CHARACTERISTICS

V_{REF} vs I_{REF} for Different Temperatures



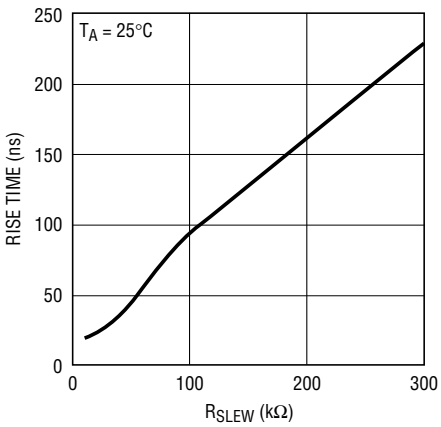
1923 G04

Output Dead Time vs R_T



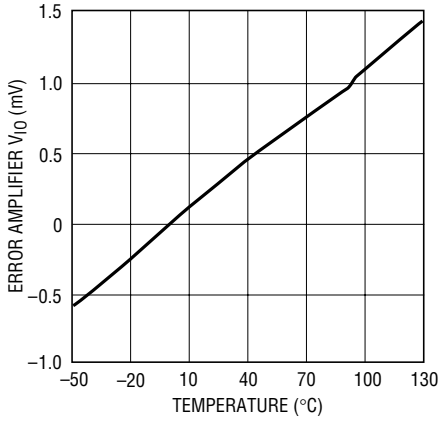
1923 G05

Output Rise/Fall Time vs R_{SLEW}



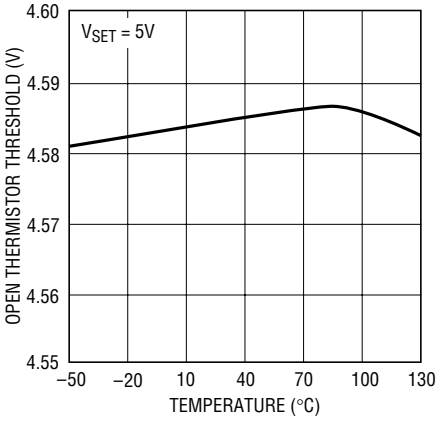
1923 G06

Error Amplifier Offset Voltage vs Temperature



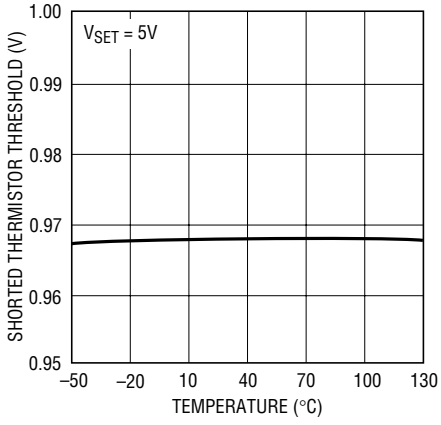
1923 G07

Open Thermistor Threshold vs Temperature



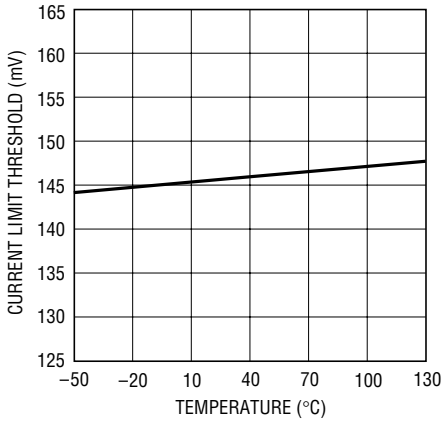
1923 G08

Shorted Thermistor Threshold vs Temperature



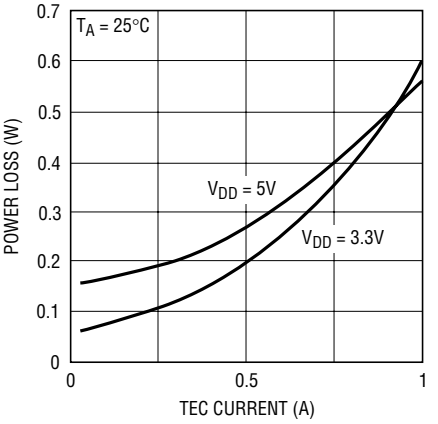
1923 G09

Current Limit Threshold vs Temperature



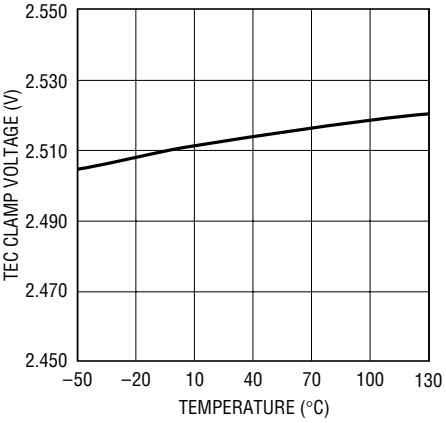
1923 G10

System Power Loss vs TEC Current



1923 G11

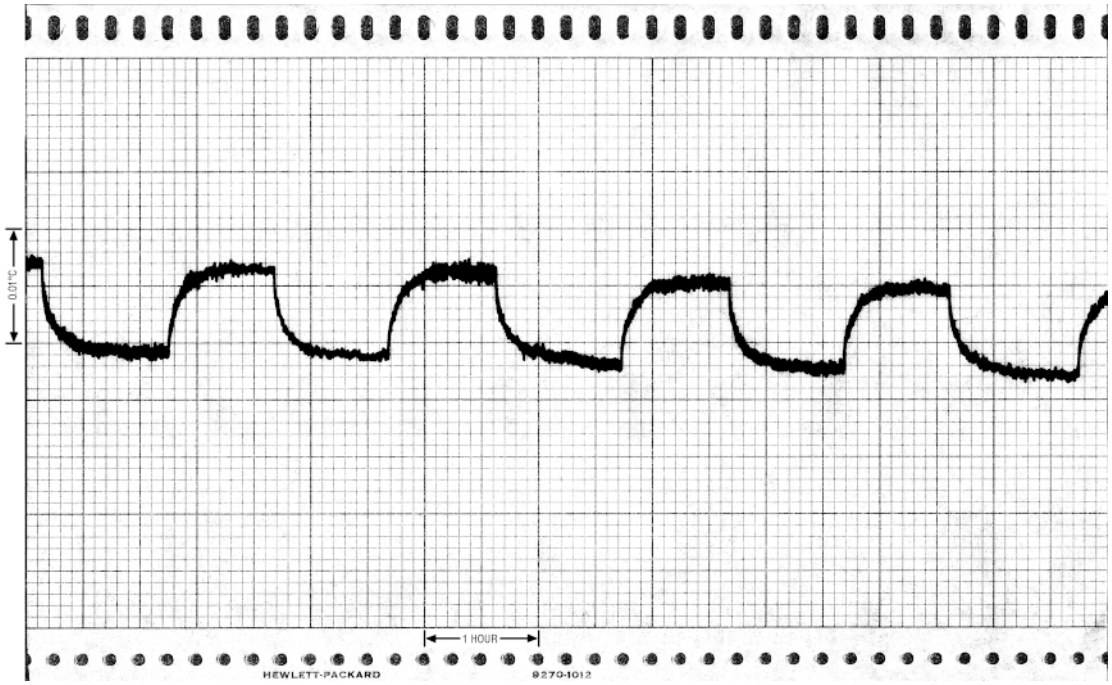
TEC Clamp Voltage vs Temperature



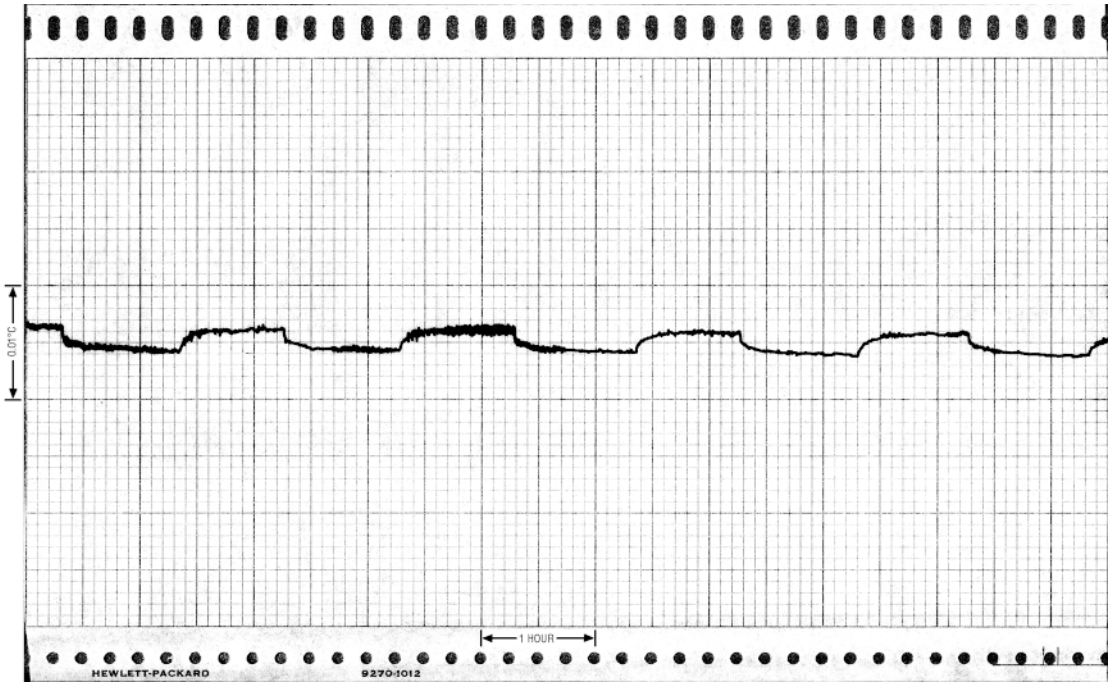
1923 G12

TYPICAL PERFORMANCE CHARACTERISTICS

Long-Term Cooling Mode Stability Measured in Environment that Steps 20 Degrees Above Ambient Every Hour. Data Shows Resulting 0.008°C Peak-to-Peak Variation, Indicating Thermal Gain of 2500. 0.0025°C Baseline Tilt Over Plot Length Derives From Varying Ambient Temperature



Identical Test Conditions as Above, Except in Heating Mode. TEC's Higher Heating Mode Efficiency Results in Higher Thermal Gain. 0.002°C Peak-to-Peak Variation Is 4x Stability Improvement. Baseline Tilt, Just Detectable, Shows Similar 4x Improvement vs Above



PIN FUNCTIONS

PLLLPF (Pin 1): This pin serves as the lowpass filter for the phase-locked loop when the part is being synchronized. The average voltage on this pin equally alters both the oscillator charge and discharge currents, thereby changing the frequency of operation. Bringing the voltage on this pin above V_{DD} – 0.4V signifies that the part will be used as the synchronization master. This allows multiple devices on the same board to be operated at the same frequency. The SDSYNC pin will be pulled low during each C_T charging cycle to facilitate synchronization.

R_{SLEW} (Pin 2): Placing a resistor from this pin to AGND sets the voltage slew rate of the output driver pins. The minimum resistor value is 10k and the maximum value is 300k. Slew rate limiting can be disabled by tying this pin to V_{DD}, allowing the outputs to transition at their maximum rate.

$\overline{\text{SDSYNC}}$ (Pin 3): This pin can be used to disable the IC, synchronize the internal oscillator or be the master to synchronize other devices. Grounding this pin will disable all internal circuitry and cause NDRVA and NDRVB to be forced low and PDRVA and PDRVB to be forced to V_{DD}. EAOUT will be forced low. $\overline{\text{FAULT}}$ will also be asserted low indicating a fault condition. The pin can be pulled low for up to 20µs without triggering the shutdown circuitry. The part can either be slaved to an external clock or can be used as the master (see Applications Information for a more detailed explanantion).

CNTRL (Pin 4): Noninverting Input to the Error Amplifier.

EAOUT (Pin 5): Output of the Error Amplifier. The loop compensation network is connected between this pin and FB. The voltage on this pin is the input to the PWM comparator and commands anywhere between 0% and 100% duty cycle to control the temperature of the temperature sense element.

FB (Pin 6): The Inverting Input to the Error Amplifier. This input is connected to EAOUT through a compensating feedback network.

AGND (Pin 7): Signal Ground. All voltages are measured with respect to AGND. Bypass V_{DD} and V_{REF} with low ESR capacitors to the ground plane near this pin.

SS (Pin 8): The TEC current can be soft-started by adding a capacitor from this pin to ground. This capacitor will be charged by a 1.5µA current source. This pin connects to one of the inverting inputs of the current limit comparator and allows the TEC current to be linearly ramped up from zero. The voltage on this pin must be greater than 1.5V to allow the open/shorted thermistor window comparitor to signal a fault.

I_{LIM} (Pin 9): A voltage divider from V_{REF} to this pin sets the current limit threshold for the TEC. If the voltage on this pin is set higher than 1V, then I_{LIM} = 150mV/R_S as that is the internal current limit comparator level. If the voltage on this pin is set less than 1V, the current limit value where the comparator trips is:

$$I_{LIM} = [0.15 \bullet R_{ILIM1} \bullet V_{REF}]/[(R_{ILIM1} + R_{ILIM2}) \bullet R_S]$$

V_{SET} (Pin 10): This is the input for the setpoint reference of the temperature sense element divider network or bridge. This pin must be connected to the bias source for the thermistor divider network.

$\overline{\text{FAULT}}$ (Pin 11): Open-drain output that indicates by pulling low when the voltage on V_{THRM} is outside the specified window, the part is in shutdown, undervoltage lockout (UVLO), or the reference is not good. When the voltage on V_{THRM} is outside the specified window, it signifies that the thermistor impedance is out of its acceptable range. This signal can be used to flag a microcontroller to shut the system down or used to disconnect power from the bridge. See Applications Information for using this signal for redundant protection.

V_{THRM} (Pin 12): Voltage Across the Thermistor. If the voltage on this pin is outside the range between 350mV below V_{SET} and 0.2 • V_{SET}, the $\overline{\text{FAULT}}$ pin will be asserted (and latched) low indicating that the thermistor temperature has moved outside the acceptable range.

H/C (Pin 13): This open-drain output provides the direction information of the TEC current flow. If TEC^+ is greater than TEC^-, which typically corresponds to the system cooling, this output will be a logic low. If the opposite is the case, this pin will pull to a logic high.

PIN FUNCTIONS

V_{TEC} (Pin 14): Output of the differential TEC voltage amplifier equal to the magnitude of the voltage across the TEC.

TEC⁻ (Pin 15): Inverting Input to the Differential TEC Voltage Amplifier. This amplifier has a fixed gain of 1 with its output being the voltage across the TEC with respect to AGND. This input, along with TEC⁺, signifies whether the TEC is heating or cooling the laser as indicated by the H/C pin.

TEC⁺ (Pin 16): Noninverting Input to the Differential TEC Voltage Amplifier.

I_{TEC} (Pin 17): Output of the Differential Current Sense Amplifier. The voltage on this pin is approximately equal to $10 \bullet I_{TEC} \bullet R_S$, where I_{TEC} is the thermoelectric cooler current and R_S is the sense resistor used to sense this current. This voltage represents only the magnitude of the current and provides no direction information. Current limit occurs when the voltage on this pin exceeds the lesser of 1.5 times the voltage on SS, 1.5 times the voltage on I_{LIM} or 1.5V. When this condition is present, the pair of outputs, which are presently conducting, are immediately turned off. The current limit condition is cleared when the C_T pin reaches the next corresponding peak or valley (see Current Limit section).

CS⁻ (Pin 18): Inverting Input to the Differential Current Sense Amplifier.

CS⁺ (Pin 19): Noninverting Input of the Differential Current Sense Amplifier. The amplifier has a fixed gain of 10.

PDRVA, PDRVB (Pins 20, 25): These push-pull outputs are configured to drive the opposite high side PMOS switches in a full-bridge arrangement.

NDRVA, NDRVB (Pins 21, 24): These push-pull outputs are configured to drive the opposite low side switches in a full-bridge arrangement.

PGND (Pin 22): This is the high current ground for the IC. The external current sense resistor should be referenced to this point.

V_{DD} (Pin 23): Positive Supply Rail for the IC. Bypass this pin to PGND and AGND with > 10µF low ESL, ESR ceramic capacitors. The turn on voltage level for V_{DD} is 2.6V with 130mV of hysteresis.

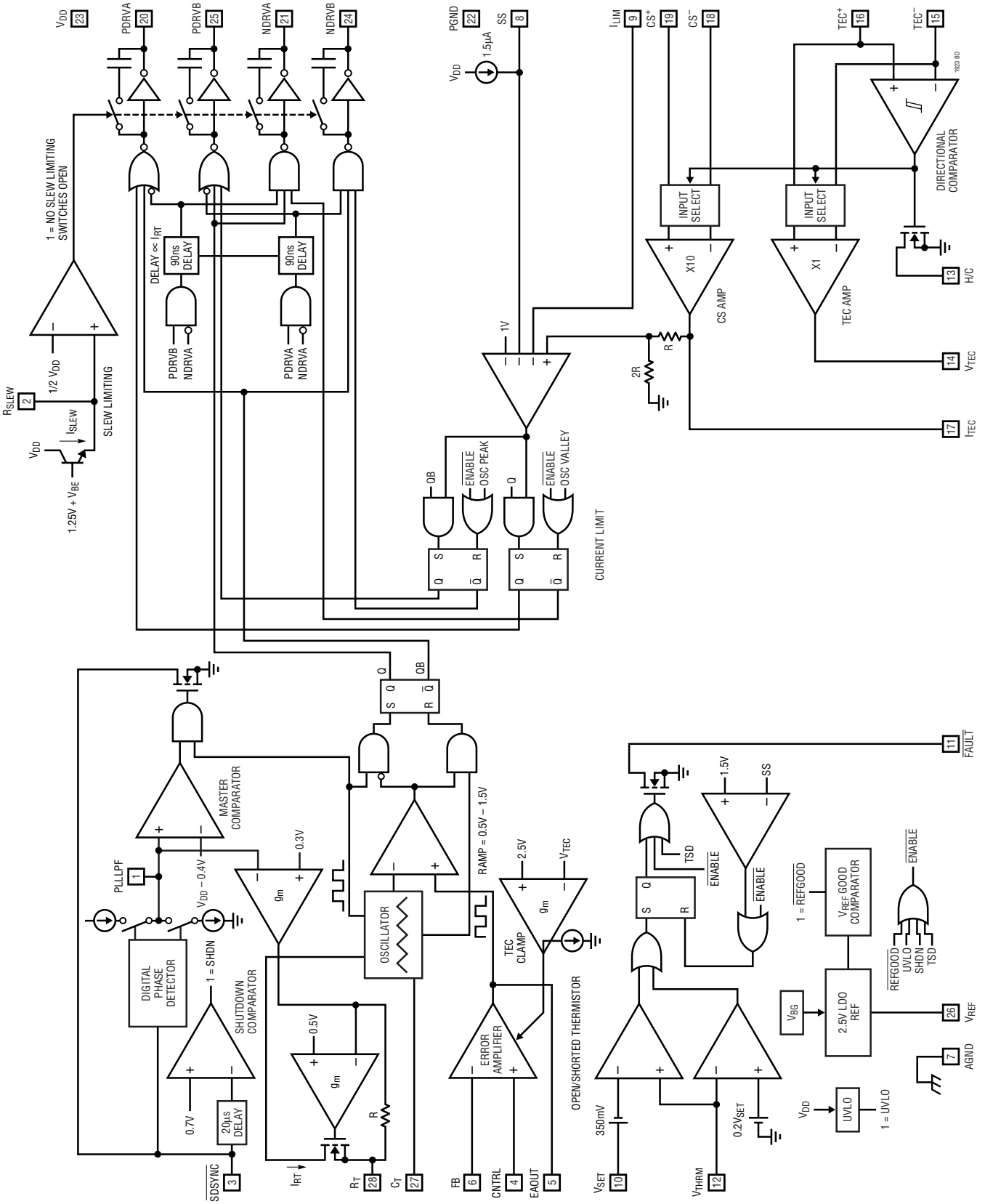
V_{REF} (Pin 26): This is the output of the Reference. This pin should be bypassed to GND with a 1µF ceramic capacitor. The reference is able to supply a minimum of 10mA of current and is internally short-circuit current limited.

C_T (Pin 27): The triangular wave oscillator timing capacitor pin is used in conjunction with R_T to set the oscillator frequency. The equation for calculating frequency is:

$$f_{OSC} = \frac{0.75}{R_T \bullet C_T} Hz$$

R_T (Pin 28): A single resistor from R_T to AGND sets the charging and discharging currents for the triangle oscillator. This pin also sets the dead time between turning one set of outputs off and turning the other set on to ensure the outputs do not cross conduct. The voltage on this pin is regulated to 0.5V. For best performance, the current sourced from the R_T pin should be limited to a maximum 150µA. Selecting R_T to be 10k is recommended and provides 90ns of dead time.

FUNCTIONAL DIAGRAM



OPERATION

MAIN CONTROL LOOP

The LTC1923 uses a constant frequency, voltage mode architecture to control temperature. The relative duty cycles of two pairs of N-/P-channel external MOSFETs, set up in a full-bridge (also referred to as an H-bridge) configuration are adjusted to control the system temperature. The full-bridge architecture facilitates bidirectional current flow through a thermoelectric cooler (TEC) or other heating element. The direction of the current flow determines whether the system is being heated or cooled. Typically a thermistor, platinum RTD or other appropriate element is used to sense the system temperature. The control loop is closed around this sense element and TEC.

The voltage on the output of the error amplifier, EAOUT, relative to the triangle wave on C_T, controls whether the TEC will be heating or cooling. A schematic of the external full bridge is shown in Figure 1. The "A" side of the bridge is comprised of the top left PMOS, MPA, and lower right NMOS, MNA. The gates of these devices are attached to the PDRVA and NDRVA outputs of the LTC1923, respectively. The "B" side of the bridge is comprised of PMOS, MPB and NMOS, MNB. The gates of these MOSFETs are controlled by the PDRVB and NDRVB outputs of the LTC1923.

The "A" side of the bridge is turned on (NDRVA is high and PDRVA is low) when the output of the error amplifier is less than the voltage on the C_T pin as shown in Figure 2.

For this condition, the state of each output driver is as follows: PDRVA is low, NDRVA is high, PDRVB is high and NDRVB is low. When the voltage on EAOUT is greater than the voltage on the C_T pin, the "B" side of the bridge is turned on. The average voltage across the TEC, $V_{TECOOLER}$, is approximately:

$$V_{TECOOLER} = V_{TEC}^{+} - V_{TEC}^{-} = V_{DD} \bullet (D_A - D_B)$$

where

V_{DD} = the full-bridge supply voltage

$V_{TECOOLER} = V_{TEC}^{+} - V_{TEC}^{-}$

D_A = the duty cycle of the "A" side of the bridge or the amount of time the "A" side is on divided by the oscillator period

D_B = the duty cycle of the "B" side of the bridge

Duty cycle terms D_A and D_B are related by the following equation:

$$D_A = 1 - D_B$$

In steady-state, the polarity of $V_{TECOOLER}$ indicates whether the system is being heated or cooled. Typically, when current flows into the TEC$^+$ side of the cooler, the system is being cooled and heated when current flows out of this terminal. *Note: Do not confuse the TEC$^+$ side of the TEC with the TEC$^+$ input of the LTC1923, although these two points should be connected together.*

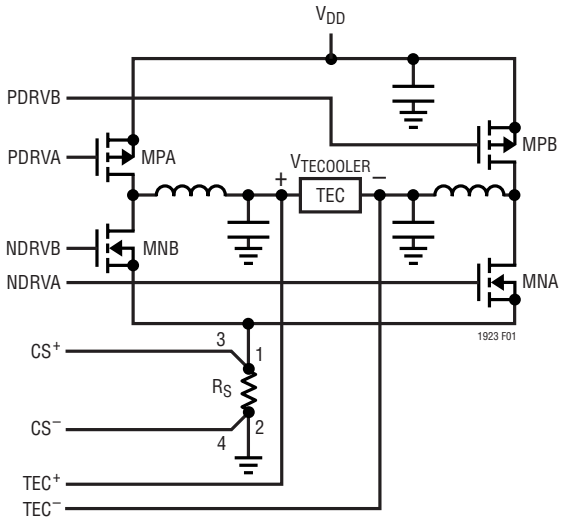


Figure 1. Full-Bridge Schematic

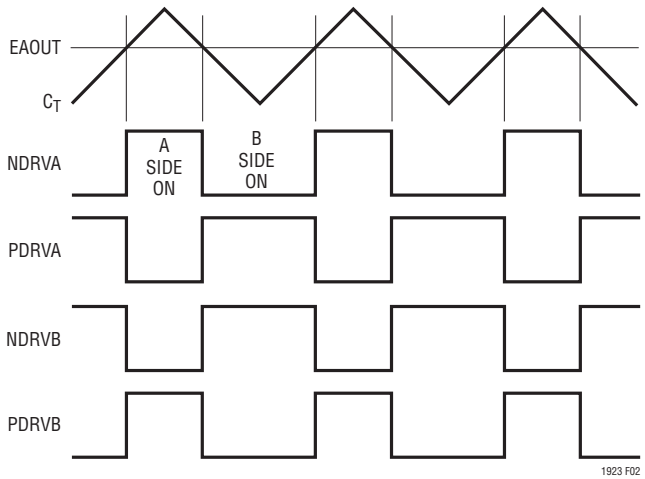


Figure 2. Error Amplifier Output, C_T and Output Driver Waveforms

OPERATION

PROTECTION FEATURES

Many protection features have been integrated into the LTC1923 to ensure that the TEC is not overstressed or the system does not thermally run away. These features include pulse-by-pulse current limiting, TEC voltage clamping and open/shorted thermistor detection.

Current Limit

The peak current in the full bridge during each switching cycle can be limited by placing a sense resistor, R_S, from the common NMOS source connections of MNA and MNB to ground. The CS^+ and CS^- connections should be made as shown in Figure 1. Current limit is comprised of a fixed gain of ten differential amplifier, an attenuator (resistor divider) and a current limit comparator. A detailed diagram of the circuitry is shown in Figure 3. The differential amplifier output, I_{TEC}, is provided to allow the user the ability to monitor the instantaneous current flowing in the bridge. If an average current is desired, an external RC filter can be used to filter the I_{TEC} output. Approximately 50ns of leading edge blanking is also internally integrated to prevent nuisance tripping of the current sense circuitry. It relieves the filtering requirements for the CS input pins.

During a switching cycle, current limit occurs when the voltage on I_{TEC} exceeds the lowest of the following three conditions: 1) 1.5 times the voltage on the SS pin, 2) 1.5 times the voltage on the I_{LIM} pin or 3) 1.5V. When a current limit condition is sensed, all four external FETs are immediately shut off. These devices are turned back on only after C_T reaches the same state (either charging or discharging) as when the current limit condition occurred. For instance, if C_T is charging when current limit occurs, the outputs are forced off for the remainder of this charging time, the entire C_T discharge time, and are only re-enabled when C_T reaches its valley voltage and begins charging again. An analogous sequence of events occurs if current limit is tripped while C_T is being discharged.

The full-bridge current can be soft-started (gradually increased) by placing a capacitor from the SS pin to ground. A 1.5μA current is sourced from the chip and will charge the capacitor. This limits the inrush current at start-up and allows the current delivered to the TEC to be linearly increased from zero.

The LTC1923 features a dedicated pin, I_{LIM}, to adjust current limit. If the voltage placed on I_{LIM} is greater than 1V, the default current limit, I_{LIMIT}, is:

$$I_{LIMIT} = 150mV/R_S$$

where R_S = the current sense resistor.

Utilizing the I_{LIM} pin allows the current limit threshold to be easily set and adjusted (the current limit threshold can also be adjusted by changing R_S). More importantly, it facilitates independent setting of the heating and cooling current limits with the addition of one transistor. Figure 4 shows how to implement this using three resistors and an external NMOS, M1. In many applications, a higher cooling capability is desired. When TEC^+ is greater than TEC^-, the H/C output is in a low state signifying that the system is being cooled (this is typical for most lasers).

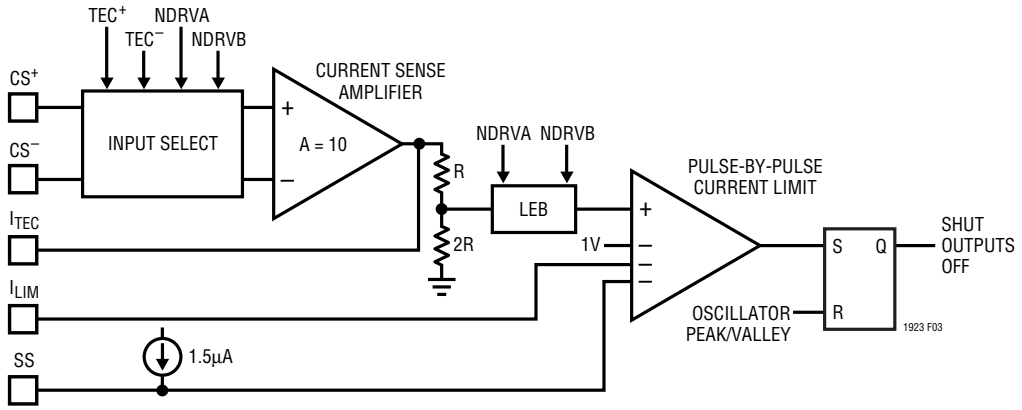


Figure 3. Current Sense Circuitry

OPERATION

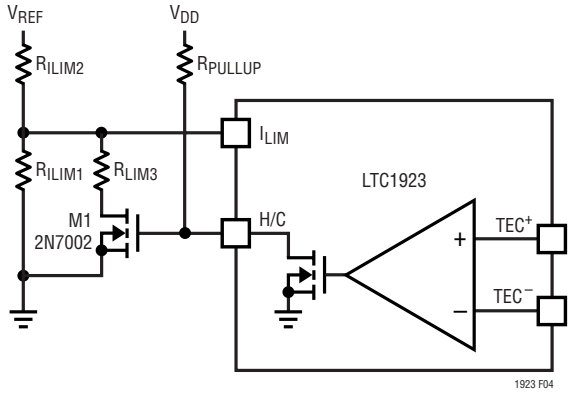


Figure 4. Independently Heating/Cooling Current Limit

Transistor M1 is off and the current limit threshold is given by:

$$I_{LIMIT} = \frac{0.15 \bullet R_{ILIM1} \bullet V_{REF}}{(R_{ILIM1} + R_{ILIM2}) \bullet R_S}$$

When TEC$^-$ is greater than TEC$^+$, the open-drain output, H/C, pulls high through R_{PULLUP}, causing M1 to turn on.

The current limit value is given by:

$$I_{LIMIT} = \frac{0.15 \bullet (R_{ILIM1} \| R_{ILIM3}) \bullet V_{REF}}{(R_{ILIM2} + R_{ILIM1} \| R_{ILIM3}) \bullet R_S}$$

reducing the current limit threshold for heating. If the heating current limit needs to be greater than the cooling limit, an extra inversion can be added.

Open/Shorted Thermistor Detection

The temperature sense element (NTC thermistor, platinum RTD or other appropriate component) must be properly connected in order for the system to regulate temperature. If the sense element is incorrectly connected, the system will be unable to control the temperature and the potential exists for the system to thermally run away.

A TEC by nature produces a temperature differential between opposite sides of the device depending upon how much current is flowing through it. There is a maximum limit to the amount of temperature differential that can be produced, which depends upon a number of physical parameters including the size of the TEC and how well heatsinked the device is. The TEC itself dissipates power to produce the temperature differential, generating heat, which must also be removed. At a certain level of power dissipation in the TEC, both sides will begin to heat. This is because the TEC will not be able to pump the self-generated heat to the outside world, which can lead to thermal runaway. If the device thermally runs away, damage to the TEC and possibly the components whose temperature is being regulated will occur.

The LTC1923 contains two dedicated comparators that directly monitor the voltage on the thermistor. If this voltage is outside the valid window, a latch is set and the $\overline{FAULT}$ pin is asserted low. The output drivers are **not** shut off and the control circuitry is not disabled, meaning the part **will continue** to try to regulate temperature. It is up to the user to use the $\overline{FAULT}$ signal to disable the appropriate circuitry. There are a couple of ways to do this. The first way is to have the $\overline{FAULT}$ signal a system microprocessor to shut the system down through the $\overline{SDSYNC}$ pin. Figure 5 shows another means of protecting the system. External NMOS M1 and PMOS M2 have been added along with two pull-up resistors (RP1 and RP2). M1 and RP2 invert the $\overline{FAULT}$ signal while M2 acts as a switch in series with bridge. When no fault is present, the gate of M1 is

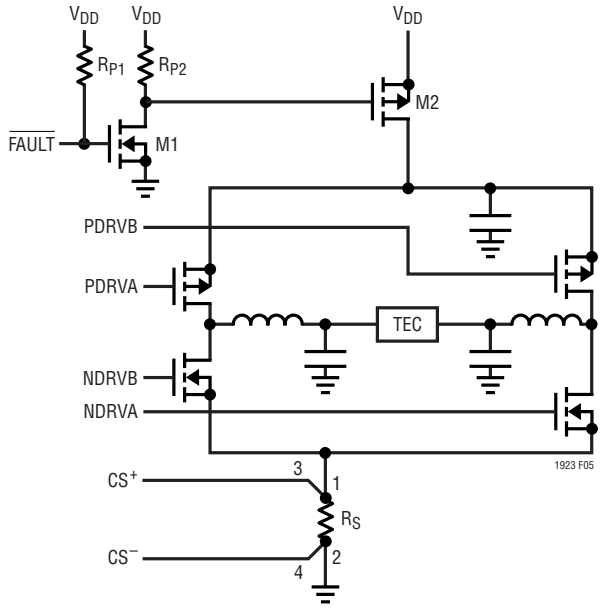


Figure 5. Redundant Fault Protection

OPERATION

pulled to V_{DD} forcing the gate of M2 low, which allows the bridge to operate as described earlier. When a fault occurs and FAULT is asserted low, M1 is shut off, forcing the gate of M2 high, shutting that device off. The power path is thus opened, ensuring no current is delivered to the TEC. M2 wants to have low $R_{DS(ON)}$ (less than the value of R_S to minimize the power losses associated with it). R_{P1} and R_{P2} can be selected on the order of 100k.

The lower comparator threshold level is 20% (twenty percent) of V_{SET} and the upper comparator threshold level is 350mV below V_{SET}, where V_{SET} is the voltage applied on the V_{SET} pin. V_{SET} is typically tied to the bias source for the thermistor divider so that any variations will track out.

The V_{SET} pin has a high input impedance so that a divided-down voltage can be supplied to this pin to modify the acceptable thermistor impedance range. This is shown in Figure 6. The voltage applied to the V_{SET} pin must be a minimum of 2V. The lower thermistor impedance threshold is:

$$R_{TH(LOWER)} = \frac{0.2 \bullet R1 \bullet R3}{R2 + 0.8 \bullet R3}$$

The upper impedance threshold is:

$$R_{TH(UPPER)} = \frac{R1\left(R3 - \alpha(R2 + R3)\right)}{R2 + \alpha(R2 + R3)}$$

where $\alpha = 0.35/V_{SET}$.

Changing R1 also changes the valid thermistor impedance range.

Example: $V_{REF} = V_{SET} = 2.5V$

R1 = 10k, R2 = 0Ω, R3 = open

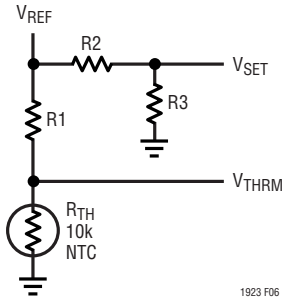


Figure 6. Modifying the Acceptable Thermistor Range

R_{TH} = 10k NTC thermistor with a temperature coefficient of –4.4%/C at 25°C.

The acceptable thermistor impedance range before causing a fault is 2.5kΩ to 61kΩ. This corresponds to a valid temperature range of between about –10°C and 60°C.

To ensure the part does not power up into a FAULT at start-up, a FAULT will not be latched until soft-start has completed. This corresponds to the voltage on SS reaching 1.5V. For a 1µF soft-start capacitor, this delay is approximately 1 second. This provides enough time for all supplies (V_{DD}, setpoint reference and V_{REF}) to settle at their final values.

TEC Voltage Clamping

An internal clamp circuit is included to protect the TEC from an overvoltage condition. When the differential voltage across the TEC exceeds 2.5V, the error amplifier output voltage at the input of the PWM comparator is limited. This clamps the duty cycle of the output drivers, and therefore, the voltage across the TEC. The voltage where clamping occurs can be increased by placing a resistor divider in parallel with the TEC and by making the appropriate connections to TEC^+ and TEC^- as shown in Figure 7. The divider increases the voltage across the TEC, $V_{TECOOLER}$, where the clamp activates, to:

$$V_{TECOOLER} = \frac{\left(1 + \frac{R_{TE1}}{R_{TE2}} + \frac{R_{TE1}}{100k}\right) \bullet 2.5 - V_{CM}\left(\frac{R_{TE1}}{200k}\right)}{1 + \frac{R_{TE1}}{200k}}$$

The terms containing the fixed resistance values are the loading errors introduced by the input impedance of the differential amplifier. A common mode voltage error is also introduced since the addition of R_{TE1} and R_{TE2} change the fully differential nature of the amplifier. In order to

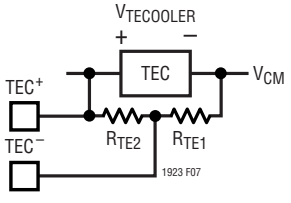


Figure 7. Increasing Voltage Clamp Threshold

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minimize these errors select R_{TE1} and R_{TE2} to be 10k or less. The above equation reduces to:

$$V_{TECOOLER} \cong \left(1+\frac{R_{TE1}}{R_{TE2}}\right)2.5$$

The Higher Voltage Applications section shows a fully differential means to increase the clamp voltage.

This will similarly alter the heating and cooling direction thresholds by the same factor, increasing the thresholds to (R_{TE1} and R_{TE2} are assumed to be ≤10k):

$$DIRH = 50mV\left(1+\frac{R_{TE1}}{R_{TE2}}\right)$$

$$DIRL = -50mV\left(1+\frac{R_{TE1}}{R_{TE2}}\right)$$

The output voltage on the VTEC pin, V_{VTEC}, will be reduced by the same ratio:

$$V_{VTEC} = \frac{V_{TECOOLER}}{1+\frac{R_{TE1}}{R_{TE2}}}$$

Oscillator Frequency

The oscillator determines the switching frequency and the fundamental positioning of all harmonics. The switching frequency also affects the size of the inductor that needs to be selected for a given inductor ripple current (as opposed to TEC ripple current which is a function of both the filter inductor and capacitor). A higher switching frequency allows a smaller valued inductor for a given ripple current. The oscillator is a triangle wave design. A current defined by external resistor R_T is used to charge and discharge the capacitor C_T. The charge and discharge rates are equal. The selection of high quality external components (5% or better multilayer NPO or X7R ceramic capacitor) is important to ensure oscillator frequency stability.

The frequency of oscillation is determined by:

$$f_{OSC(kHz)} = 750 \bullet 10^6/[R_T(k\Omega) \bullet C_T(pF)]$$

The LTC1923 can run at frequencies up to 1MHz. The value selected for R_T will also affect the delay time between one side of the full bridge turning off and the opposite side turning on. This time is also known as the "break-before-make" time. The typical value of 10kΩ will produce a 90ns "break-before-make" time. For higher frequency applications, a smaller value of R_T may be required to reduce this delay time. For applications where significant slew rate limiting or external gate driver chips are used, a higher value for R_T may necessary, increasing the dead time. The "break-before-make" time can be approximately calculated by:

$$t_{DELAY} = R_T\,(k\Omega) \bullet 5.75 \bullet 10^{-9} + 35ns$$

Phase-Locked Loop

The LTC1923 has an internal voltage-controlled oscillator (VCO) and phase detector comprising a phase-locked loop. This allows the oscillator to be synchronized with another oscillator by slaving it to a master through the $\overline{SDSYNC}$ pin. The part can also be designated as the master by pulling the PLLLPF pin high to V_{DD}. This will result in the part toggling the $\overline{SDSYNC}$ pin at its set oscillator frequency. This signal can then be used to synchronize additional oscillators.

When being slaved to another oscillator, the frequency should be set 20% to 30% lower than the target frequency. The frequency lock range is approximately ±50%.

The phase detector is an edge sensitive digital type, which provides zero degrees phase shift between the external and internal oscillators. This detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The VCO hold-in range is equal to the capture range dfH = dfC = $\pm 0.5f_O$.

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLLPF pin. A simplified block diagram is shown in Figure 8.

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency, current is sourced continuously out of the PLLLPF pin. When the external frequency is less than the oscillator frequency, current is sunk by the PLLLPF pin. The loop filter components R_{LP}, C_{LP} and C_{LP2}, smooth out

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current pulses from the phase detector and provide a stable input to the VCO. These components also determine how fast the loop acquires lock. In most instances C_{LP} can be omitted, R_{LP} can be set to 1k and C_{LP2} can be selected to be 0.01µF to 0.1µF to stabilize the loop. Make sure that the low side of filter components is tied to AGND to keep unwanted switching noise from altering the performance of the PLL.

As mentioned earlier, one LTC1923 can be used as a master to synchronize other LTC1923s or additional devices requiring synchronization. To implement this, determine the values of R_T and C_T to obtain the desired free-running oscillator frequency of the master by using the equation given in the oscillator frequency section. Tie the PLLLPF pin of the master to V_{DD} through a resistor R_{PLL} as shown in Figure 8. R_{PLL} typically can be set to 10k, but may need to be less if higher frequency operation is desired (above 250kHz). Set the slave free-running frequencies to be 20% to 30% less than this. The $\overline{SDSYNC}$ pin of the master will switch at its free-running frequency (with approximately 50% duty cycle), and this can be used to synchronize the other devices.

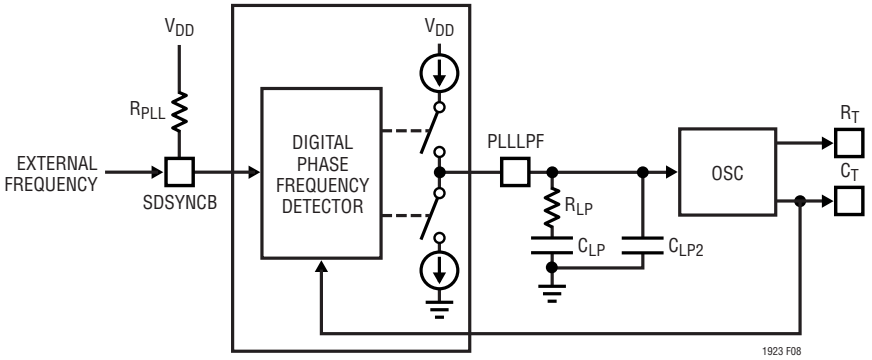

Figure 8. Phase-Locked Loop Block Diagram

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The thermistor may be isolated from the control circuitry. It has a relatively high input impedance and is therefore susceptible to noise pick up. Extreme care should be taken to ensure this signal is noise free by shielding the line (coaxially). A lowpass filter can be added between the thermistor and the input to the LTC2053, but since it is in the signal path, there are limitations on how much can be added.

Inductor Ripple Current

The current that flows in the bridge can be separated into two components, the DC current that flows through the TEC and the inductor ripple current that is present due to the switchmode nature of the controller. Although the TEC current has its own ripple component, proper filtering will minimize this ripple relative to the inductor ripple current, validating this assumption that the TEC current is constant (see TEC Ripple Current section). A simplified half-circuit of the bridge in steady-state is shown in Figure 9. The current, I_L, through the inductor (L) consists of the ripple current (ΔI_1) and static TEC current (I_{TEC}). The ripple current magnitude, ΔI_1, can be calculated using the following equation:

$$\Delta I_1 = (V_{BRIDGE}^2 - V_{TEC}^2)/(4 \bullet f_{OSC} \bullet L \bullet V_{BRIDGE})$$

where

V_{BRIDGE} is the full-bridge supply voltage (typically V_{DD})

f_{OSC} is the oscillator frequency

L is the filter inductor value

V_{TEC} is the DC voltage drop across the TEC

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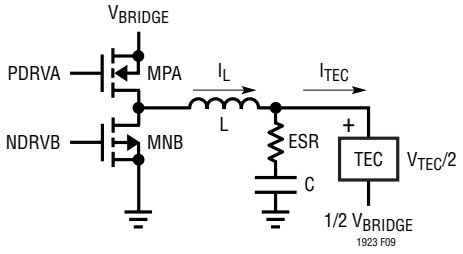

Figure 9. Full-Bridge Half Circuit

The peak inductor current is equal to $I_{TEC} + \Delta I_1/2$ and is the current level that trips the current limit comparator. Keeping the ripple current component small relative to I_{TEC} keeps the current limit trip level equal to the current flowing through the TEC.

Example: V_{BRIDGE} = 5V, R_{TEC} = 2.5Ω, V_{TEC} = 2.5V, I_{TEC} = 1A, L = 22µH, f_{OSC} = 250kHz. The peak-to-peak ripple current using the above equation is:

ΔI_1 = 170mA

The peak inductor current is therefore 1.085A in order to get 1A of DC TEC current.

TEC Ripple Current

Every TEC has a fundamental limitation (based mainly on the TEC's physical characteristics) on the maximum temperature differential that it can create between sides. The ability to create this maximum temperature differential is affected by the amount of ripple current that flows through the device, relative to the DC component. An approximation of this degradation due to TEC ripple current is given by the following equation:

$dT/dT_{MAX} = 1/(1 + N^2)$

where:

dT is the adjusted achievable temperature differential

dT_{MAX} is the maximum possible temperature differential when the TEC is fed strictly by DC current and is typically specified by the manufacturer

N is the ratio of TEC ripple current to DC current

TEC manufacturers typically state that N should be no greater than 10%.

In this application, the bridge supply voltage, oscillator frequency and external filter components determine the amount of ripple current that flows through the TEC. Higher valued filter components reduce the amount of ripple current through the TEC at the expense of increased board area. Filter capacitor ESR along with inductor ripple current will determine the peak-to-peak voltage ripple across the TEC and therefore the ripple current since the TEC appears resistive.

The ripple current through the TEC, $I_{TEC(RIPPLE)}$, is approximately equal to:

$$I_{TEC(RIPPLE)} \cong \frac{V_{BRIDGE}^2 - V_{TEC}^2}{16 \bullet f_{OSC}^2 \bullet L \bullet C \bullet R_{TEC} \bullet V_{BRIDGE}} + \frac{\left(V_{BRIDGE}^2 - V_{TEC}^2\right) \bullet ESR}{2 \bullet f_{OSC} \bullet L \bullet V_{BRIDGE} \bullet R_{TEC}}$$

where:

f_{OSC} = the oscillator frequency

L = the filter inductor value

C = the filter capacitor value

R_{TEC} = the resistance of the TEC

V_{TEC} = the DC voltage drop across the TEC

ESR = the equivalent series resistance of the filter capacitor

V_{BRIDGE} = the full-bridge supply voltage typically equal to V_{DD}

The equation above shows that there are two components, which comprise TEC ripple current. The first term is the increase in voltage from the charging of the filter capacitor. The second term is due to the filter capacitor ESR and is typically the dominant contributor. Therefore the filter capacitor selected wants to have a low ESR. This capacitor can be made of multilevel ceramic, OS-CON electrolytic or other suitable capacitor. Increasing the oscillator frequency will also reduce the TEC ripple current since both terms have an inverse relationship to operating frequency.

Example: V_{BRIDGE} = 5V, R_{TEC} = 2.5Ω, V_{TEC} = 2.5V, L = 22µH, C = 22µF, f_{OSC} = 250kHz, ESR = 100mΩ

$I_{TEC(RIPPLE)}$ = 3.1mA + 13.6mA = 16.7mA

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For this example the DC current flowing through the TEC is 1A, making the ripple current equal to approximately 1.7% (this illustrates why I_{TEC} can be approximated to be DC).

Closing the Feedback Loop

Closing the feedback loop around the TEC and thermistor (or other temperature sensitive element) involves identifying where the thermal system's poles are located and placing electrical pole(s) (and zeroes) to stabilize the control loop. High DC loop gain is desirable to keep extremely tight control on the system temperature. Unfortunately the higher the desired loop gain, the larger the compensation values required to stabilize the system. Given the inherently slow time constants associated with thermal systems (on the order of many seconds), this can lead to unreasonably large component values. Therefore, the amount of loop gain necessary to maintain the desired temperature accuracy should be calculated, and after adding some margin, this should be the target DC loop gain for the system. A block diagram of the system is shown in Figure10. The gain blocks are as follows:

K_{IA} = instrumentation amplifier gain (V/V)

K_{EA} = error amplifier gain (V/V)

K_{MOD} = modulator gain (d/V)

K_{PWR} = power stage gain (V/d)

K_{TEC} = TEC gain (°C/V)

K_{THRM} = Thermistor Gain (V/°C)

K_{IA} and K_{EA} are the electrical gains associated with the instrumentation and LTC1923 error amplifier. Switching regulators are sampled systems that convert voltage to duty cycle (d), which explains why the K_{MOD} and K_{PWR} gain terms are expressed as a function of duty cycle and voltage. The TEC converts voltage to temperature change, while the thermistor's impedance and therefore voltage across it changes with temperature.

The loop gain can be expressed by the following equation:

$$T \text{ (loop gain)} = K_{IA} \bullet K_{EA} \bullet K_{MOD} \bullet K_{PWR} \bullet K_{TEC} \bullet K_{THRM}$$

And the error introduced by the finite gain of the system, V_E, can be expressed by:

$$V_E = V_{IN}/(1 + T)$$

This voltage error translates back into a temperature setpoint error.

Example:

R_{THRM} = 10k

NTC with 4.4%/°C at 25°C

R1 = 10k

V_{REF} = 2.5V

T = 25°C

For this thermistor with a 25°C temperature setpoint, the change in thermistor voltage with temperature is given by –25mV/°C. In order to maintain a 0.01°C temperature accuracy, this translates into a 250µV error signal, V_E. The

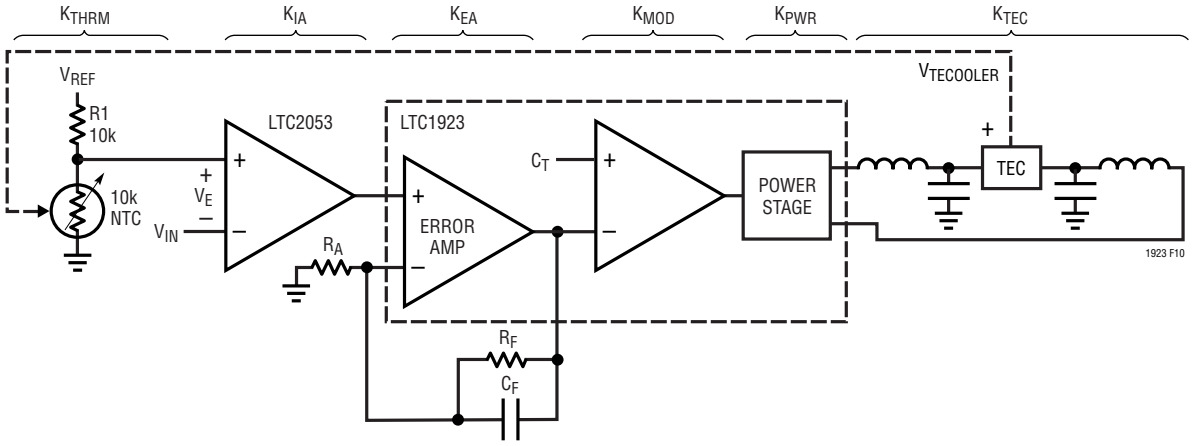

Figure 10. Simplified Loop Block Diagram

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minimum loop gain can now be calculated from the above equation:

$V_E = V_{IN}/(1 + T)$

A 25°C setpoint temperature requires V_{IN} = 1.25V for V_{REF} = 2.5V. The required loop gain is 5000 or 74dB.

There are two handles to adjust the loop gain, K_{IA} and K_{EA}, while the other handles are fixed and depend upon the TEC and thermistor characteristics (K_{TEC} and K_{THRM}), V_{SET} and R1 (K_{THRM}) and V_{DD} (K_{MOD} and K_{PWR}). The modulator and power gain product is given by:

$K_{MOD} \bullet K_{PWR} = 2 \bullet V_{DD}/V_{CT} = 2 \bullet V_{DD}$

where V_{CT} = the C_T voltage which has a fixed 1V amplitude.

The TEC gain depends upon the TEC selected and corresponds to the relationship between the voltage across the device and what temperature differential is created. This gain term changes with operating temperature, and whether the TEC is heating or cooling. TECs are inherently more efficient at heating (and therefore have a higher gain) as compared to cooling. A worst-case rough estimation of the gain can be obtained by taking the maximum TEC voltage required to force a given change in temperature from the TEC specifications:

$K_{TEC} = dT/V_{TEC(MAX)}$

The thermistor gain should be linearized around temperature setpoint.

Example:

Setpoint T = 25°C

V_{DD} = 5V

R_{THRM} = 10k NTC with 4.4%/°C at 25°C

R1 = 10k

V_{REF} = 2.5V

$dT/V_{TEC(MAX)}$ = 45°C/1.5V = 30°C/V

The linearized thermistor gain around 25°C is –25mV/°C. For a minimum loop gain of 5000 as calculated above, the combined gain of the instrumentation and error amplifiers can be calculated:

$K_{IA} \bullet K_{EA} = T/(K_{MOD} \bullet K_{PWR} \bullet K_{TEC} \bullet K_{THRM})$

$K_{IA} \bullet K_{EA} = 5000/(10 \bullet 30 \bullet 0.025) = 667$

A combined gain of 1000 can be selected to provide adequate margin. The instrumentation amplifier gain should be set at typically 10, as this attenuates any errors by its gain factor. The error amplifier gain would then be limited to the remainder through the gain setting resistors, R_F and R_A shown in Figure 10.

$R_F/R_A = KEA - 1$

The multiple poles associated with the TEC/thermistor system makes it difficult to compensate. Compounding this problem is that there will be significant variations in thermal time constants for the same system, making elaborate compensation schemes difficult to reliably implement. The most robust method (i.e., least prone to oscillation) is to place a dominant pole well below the thermal system time constant (τ) (anywhere from many seconds to minutes). This time constant will set the capacitor value by the following equation:

$C_F = \tau/R_F$

Please refer to Application Note 89 for more detailed information on compensating the loop. Ceramic capacitors are not recommended for use as the integrating capacitor or anywhere in the signal path as they exhibit a piezoelectric effect which can introduce noise into the system. The component values shown on the front page of this data sheet provide a good starting point, but some adjustment may be required to optimize the response.

Dominant pole compensation does have its limitations. It provides good loop response over a wide range of laser module types. It does not provide the fastest transient response to step changes in temperature. If this is a necessity, a more complex compensation approach as shown in Figure 11 may be required. This approach adds an additional zero into the feedback loop to speed up the transient response. First note that the LTC2053 inputs have been swapped as the LTC1923 error amplifier is now running in an inverting configuration. Capacitor C_A is needed to provide the lead term. Resistor R_C is used to buffer the LTC2053 from capacitive loading and limit the error amplifier high frequency gain.

Since the system thermal pole locations are not known, a qualitative compensation approach must be employed. This entails looking at the transient response when the

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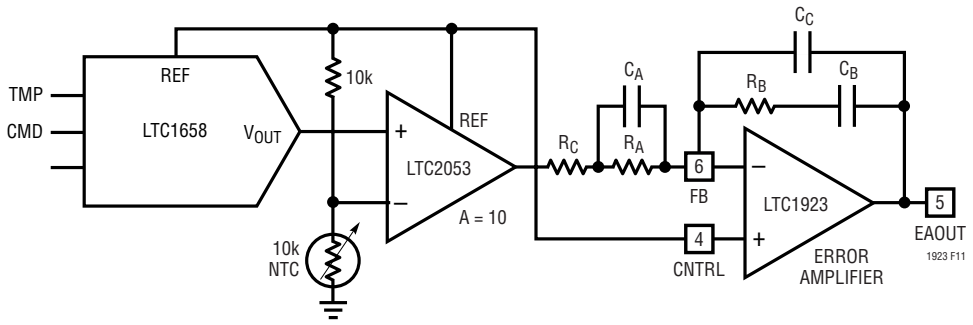

Figure 11. Alternative Compensation Method to Improve Transient Response

TEC is heating (due to the inherent higher gain) for a small-signal step change in temperature and modifying compensation components to improve the response. A reasonable starting point is to select components that mimic the response that will be obtained from the front page of this data sheet. Therefore R_A, R_B and C_B would be selected to be 1MΩ, 1MΩ and 0.47µF, respectively. R_C should be selected to be a factor of 100 smaller than R_A, or on the order of 10k. Make sure that the loop is stable prior to the introduction of capacitor C_A. The addition of C_A will provide some phase boost in the loop (in effect, offsetting one of the poles associated with the thermal system). Start with C_A on the order of C_B and note its affect on system response. Adjust the values based on observing whether the transient response was improved or not with the goal of reducing C_B to improve settling time. As the system thermal poles can vary between "identical" laser modules (i.e., same manufacturer and model), care must be taken to ensure that the values selected provide the desired response even with these thermal term variations. Compensation should also be tailored for each unique laser module as thermal terms can vary significantly between different brands. C_C rolls off high frequency gain , minimizing noise in the outputs. It is typically about 25 times smaller than C_B. C_A, C_B and C_C should be film capacitors.

Temperature Stability

It is important to differentiate between temperature accuracy and stability. Since each laser's output maximizes at some temperature, temperature setpoint is typically incremented until this peak is achieved. After this, only temperature stability is required. The predominant parameters which affect temperature stability are the thermistor, the thermistor biasing resistor and any offset drift of the front-end electrical circuitry. Sufficient loop gain ensures that any downstream variations do not contribute significantly to temperature stability. The relatively mild operating conditions inside the laser module promote good long-term thermistor stability. A high quality, low temperature coefficient resistor should be selected to bias the thermistor. If the 10k resistor has a 100ppm/°C temperature coefficient, this translates into a 0.18°C setpoint temperature differential over a 0°C to 70°C ambient for a desired 25°C laser setpoint. Depending upon the temperature stability requirements of the system, this is very significant. A lower temperature coefficient resistor may therefore be desired. The LTC2053 has maximum offset drift to 50nV/°C which translates into less than 0.001°C change for a 0°C to 70°C ambient.

The offset drift of the LTC1923 error amplifier divided by the gain of the LTC2053 also affects temperature stability. The offset drift of the LTC1923 (see characteristic curves) is typically 1mV over a 0°C to 70°C ambient. After attenuation by the LTC2053 gain, this translates into a temperature setpoint variation of 0.004°C. Neither of these offsets drifts significantly with aging. Depending upon the setpoint temperature stability requirements of the system, the LTC2053 instrumentation amplifier may not be necessary. Figure 12 shows a simplified schematic with the LTC2053 omitted.

Noise and Slew Rate Control

One disadvantage of switching regulators is that the switching creates wideband harmonic energy. The high frequency content can pose problems to associated circuitry. To combat this issue, the LTC1923 offers a pin

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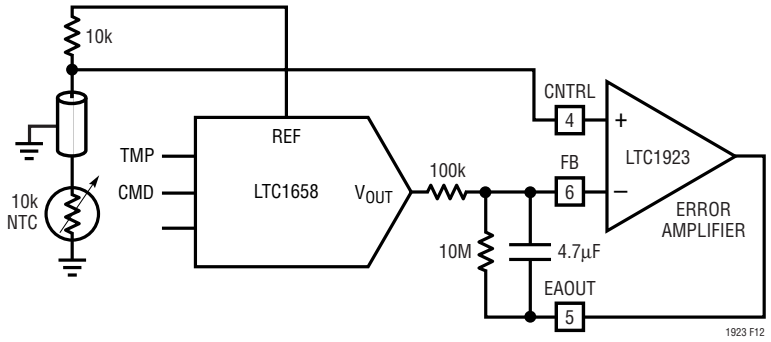

Figure 12. Simplifed Temperature Control Loop Omitting the LTC2053 Instrumentation Amplifier Front End

called R_{SLEW} that controls the slew rate of the output drive waveforms. Slowing down the transition interval reduces the harmonic frequency content by spreading out the energy over a longer time period. The additional transition time causes some efficiency loss (on the order of 2% to 3%) but significantly improves the high frequency noise reflected onto the input supply.

Slew rate control is engaged by placing a resistor from R_{SLEW} to AGND. If slew rate control is not desired, the R_{SLEW} pin should be tied to V_{DD} allowing the output drivers to transition at their fastest rate. The resistor value should be set between 10k (fastest transition) and 300k (slowest transition). This provides about a 10:1 slew rate range to optimize noise performance. The "break-before-make" time may need to be increased if slew control is implemented, especially for slower transition rates. Adjustment can be done by increasing the value of R_T (C_T can be reduced to maintain the same frequency of operation), to ensure that the bridge MOSFETs receive nonoverlapping drive.

Power MOSFET Selection

Four external MOSFETs must be selected for use with the LTC1923; a pair of N-channel MOSFETs for the bottom of the bridge and a pair of P-channel MOSFETs for the top diagonals of the bridge. The MOSFETs should be selected for their $R_{DS(ON)}$, gate charge and maximum V_{DS}, V_{GS} ratings. A maximum V_{DS} rating of 20V is more than sufficient for 5V and 12V bridge applications, but as mentioned in the High Voltage Application section, a 12V maximum V_{GS} rating is insufficient and higher voltage MOSFETs must be selected. There is a trade-off between $R_{DS(ON)}$ and gate charge. The $R_{DS(ON)}$ affects the conduction losses ($I_{TEC}^2 \bullet R_{DS(ON)}$), while gate charge is a dominant contributor to switching losses. A higher $R_{DS(ON)}$ MOSFET typically has a smaller gate capacitance and thus requires less current to charge the gate for the same BV_{DSS}. For 1A TEC applications, the Si9801DY or Si9928DY complimentary N- and P-channel MOSFETs provide a good trade-off between switching and conduction losses. Above this TEC current level the MOSFETs selected should have lower $R_{DS(ON)}$ to maintain the high end efficiency.

Efficiency Considerations

Unlike typical voltage regulators, where the output voltage is fixed, independent of load current, the output voltage of this regulator changes with load current. This is because the TEC appears resistive and the current through the TEC sets the voltage. The output power of the regulator is defined as:

$$P_{OUT} = I_{TEC}^2 \bullet R_{TEC}$$

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Often it is useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most significant improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

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For this application, the main efficiency concern is typically at the high end of output power. A higher power loss translates into a greater system temperature rise, resulting in the need for heat sinking, increasing both the system size and cost.

There are three main sources which usually account for most of the losses in the application shown on the front page of the data sheet: Input supply current, MOSFET switching losses and I^2R losses.

1) The input supply current is comprised of the quiescent current draw from the LTC1658, LTC2053, LTC1923 and any additional circuitry added. The total maximum supply current for these devices is on the order of 5mA, which gives a total power dissipation of 25mW. This power loss is independent of TEC current.

2) The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a gate is switched from low to high to low again, a packet of charge dQ moves from V_{DD} to ground. The gate charging current, $I_{GATECHG} = 2 \bullet f \bullet (Q_P + Q_N)$, where Q_P and Q_N are the total gate charges of the NMOS and PMOS on one side of the bridge, and f is the oscillator frequency. The factor of 2 arises from there being two sets of MOSFETs that make up the full bridge. Note that increasing the switching frequency will increase the dynamic current and therefore power dissipation by the same factor. This power loss is independent of TEC current.

Example: Q_N = 10nC max, Q_P = 15nC max, f = 225kHz, V_{DD} = 5V

$$\text{Power loss} = 2 \bullet f \bullet (Q_P + Q_N) \bullet V_{DD} = 56mW$$

3) The DC resistances of the external bridge MOSFETs, filter inductors and sense resistor are typically the dominant loss mechanism at the high end TEC current. The conduction path of the current includes one NMOS, one PMOS, two inductors and the sense resistor so the DC resistances associated with the components dissipate power.

Example:

$R_{DS(ON)NMOS}$ at 5V = 0.055Ω max

$R_{DS(ON)PMOS}$ at 5V = 0.08Ω max

R_S = 0.1Ω

R_L = 0.1Ω,

I_{TEC} = 1A

R_{TEC} = 2.5Ω

Total series resistance = 0.055 + 0.08 + 2 • 0.1 + 0.1
= 0.435Ω

Power Loss = $(1A)^2 \bullet 0.435\Omega = 0.435W$

Output Power = $(1A)^2 \bullet 2.5\Omega = 2.5W$

This represents a 17% efficiency loss due to conduction losses. The other two power loss mechanisms comprise a little more than a 3% efficiency loss at this output power level. This may sound alarming if electrical efficiency is the primary concern and can be easily improved by choosing lower $R_{DS(ON)}$ MOSFETs, lower series resistance inductors and a smaller valued sense resistor. If temperature rise is the primary concern, this power dissipation may be acceptable. At higher current levels, this example does illustrate that lower resistance components should be selected.

Low Voltage Requirements

All components shown on the front page of this data sheet will operate with a 2.7V input supply. Minor modifications are required to guarantee correct operation. The voltage on the REF input of the LTC2053 should be at least 1V below V_{DD}. Figure 13 shows how to implement this. By dividing down the 2.5V reference with 500Ω of impedance, feeding this to the REF input of the LTC2053 and the integrating resistor of the LTC1923 error amplifier, any common mode issues will be avoided.

APPLICATIONS INFORMATION

Higher Voltage Applications

A bank of TECs can be wired in series to minimize board real estate utilized by the application. A higher voltage supply may be required depending upon how many TECs are placed in series and what their maximum voltage drop is. In other applications, only one high current supply may be available, with the output voltage of this supply being greater than the LTC1923's absolute maximum voltage rating. The absolute maximum input voltage for the LTC1923 is 6V. Since the current drawn by the LTC1923 is small, it can be powered from a low current, 5V (or less) supply. A 12V application for driving the full bridge is shown in Figure 14. Two LTC1693-1 high speed dual MOSFET drivers are used to step up the lower voltage produced by the LTC1923 drivers to the higher voltage levels required to drive the full bridge. The LTC1693 requires proper bypassing and grounding due to its high switching speed and large AC currents. Mount the low ESR bypass capacitors as close to the pins as possible, shortening the leads as much as possible to reduce inductance. Refer to the LTC1693 data sheet for more information. Since the LTC1693-1 low-to-high and high-to-low propagation delays are almost identical (typically 35ns), there is minimal skew introduced by the addition of these drivers. Sufficient dead time (typically 50ns) between one leg of the bridge shutting off and the other turning on, as set up by the LTC1923, will be maintained. If this dead time is insufficient, the resistor tied to the R_T pin can be increased to increase this time.

Care must be taken to ensure that the external MOSFETs are properly selected based on the maximum drain-source voltage, V_{DS}, gate-source voltage, V_{GS}, and $R_{DS(ON)}$. Many MOSFETs that have an absolute maximum V_{DS} of 20V have a maximum V_{GS} of only 12V, which is insufficient for 12V applications. Even the 14V maximum V_{GS} rating of the Si9801DY may not provide adequate margin for a 12V bridge supply voltage. Refer to Efficiency Considerations for more discussion about selecting a MOSFET with $R_{DS(ON)}$.

Two pairs of resistors, R_{T1} and R_{T2}, must be added to ensure that the absolute maximum input voltage is not exceeded on the TEC$^+$ and TEC$^-$ inputs. The maximum voltage on TEC$^+$ and TEC$^-$ must be less than the V_{DD} input supply to the LTC1923 which, for this example, is 5V. The following equation will guarantee this:

$$(1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet V_{BRIDGE} < V_{DD}$$

where V_{BRIDGE} is the supply voltage to the external bridge circuitry and V_{DD} is the input supply to the LTC1923.

These additional level shifting resistors affect some parameters in the data sheet. The direction comparator thresholds are increased to:

$$(1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet 50mV \text{ and}$$

$$(1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet -50mV$$

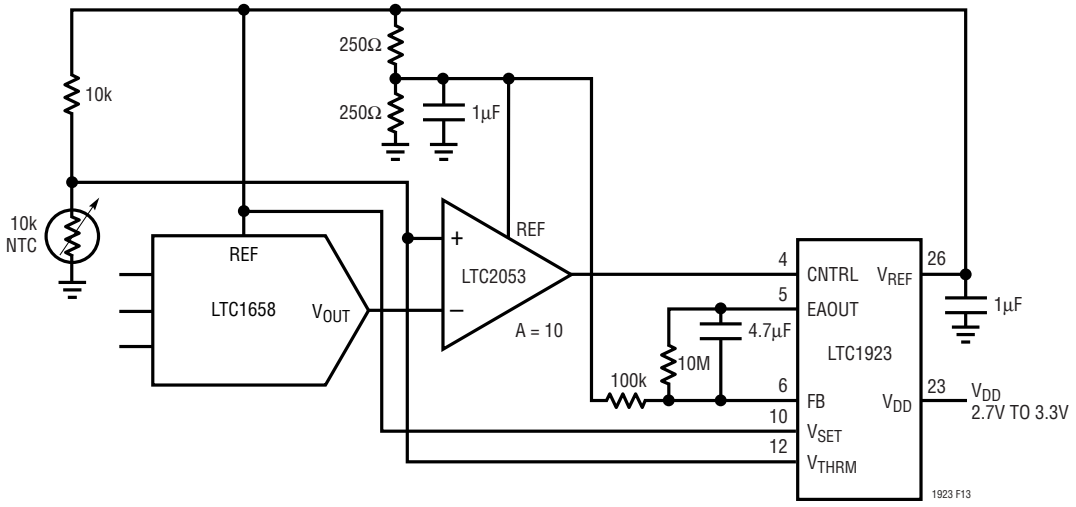


Figure 13. Low Input Supply Voltage Circuit

APPLICATIONS INFORMATION

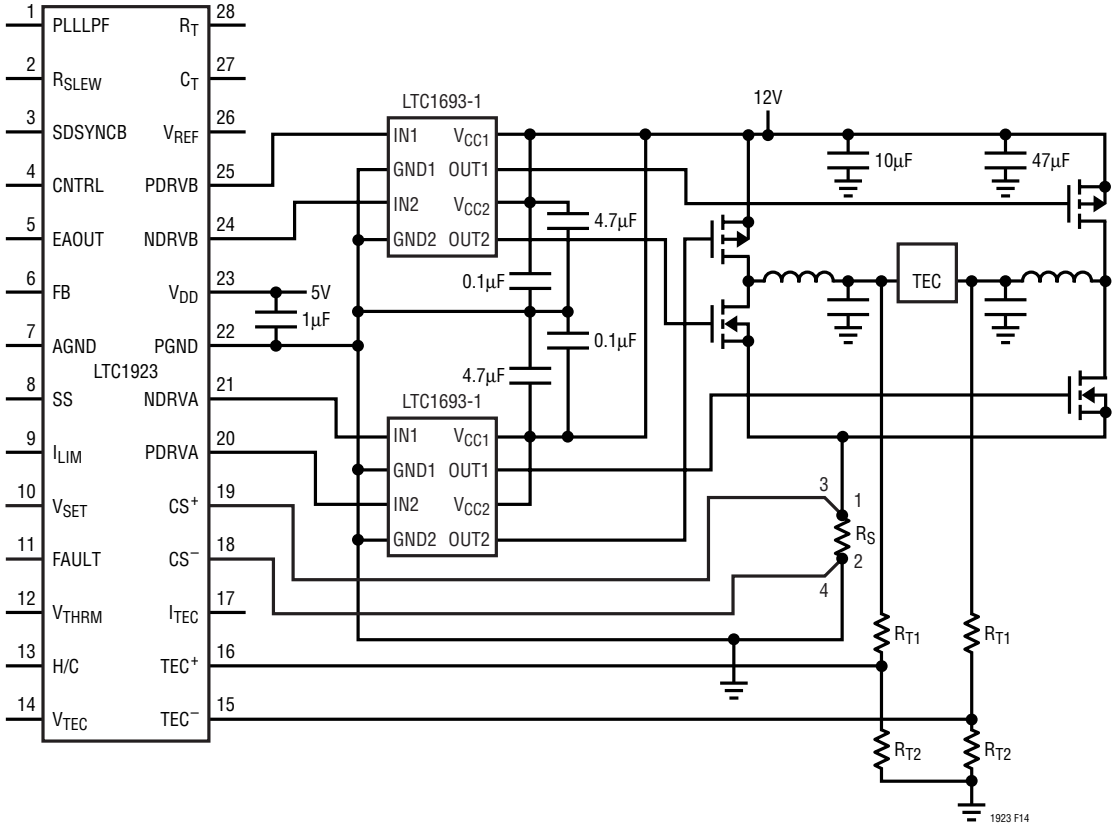


Figure 14. Higher Voltage Applications with the LTC1923

The output voltage on the V_{TEC} pin represents the voltage across the TEC ($V_{TECOOLER}$) reduced by a factor of $(1 + R_{T1}/R_{T2} + R_{T1}/100k)$ or:

$$V_{VTEC} = V_{TECOOLER}/(1 + R_{T1}/R_{T2} + R_{T1}/100k)$$

The term containing 100k is the loading error introduced by the input impedance of the differential amplifier. Typically this value will be 100k, but can vary due to normal process tolerances and temperature (up to ±30%). Due to this variability, it may be desirable to minimize the loading effect to try to keep a tight tolerance on the TEC clamp voltage. Although it will increase quiescent current draw, this can be accomplished by making the value of R_{T1} as small as possible.

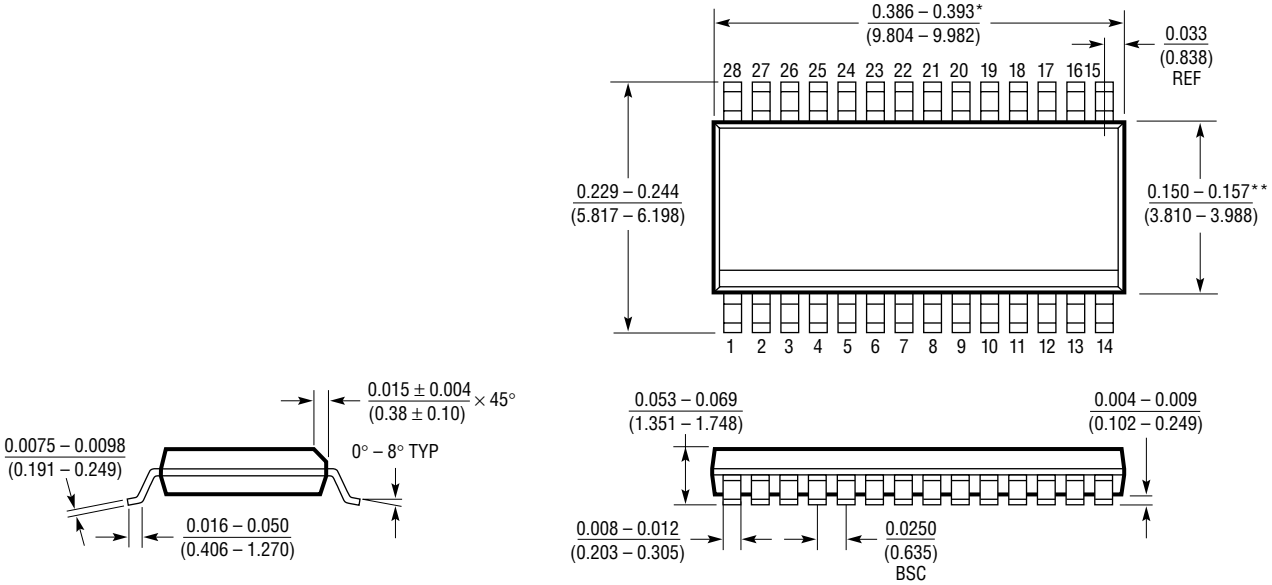
As a result of this level shifting, the TEC voltage necessary to activate the clamp is raised. The voltage across the TEC where the voltage clamp activates will be:

$$V_{TECOOLER} = (1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet 2.5V$$

One drawback with using the LTC1693 MOSFET drivers is the inability to adjust the slew rate of the output drivers to reduce system noise.

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN28 (SSOP) 1098

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1658	14-Bit Rail-to-Rail Micropower DAC	3V or 5V Single Supply Operation, I_{CC} = 270μA, 8-Lead MSOP Package
LTC1693-1	High Speed Dual N-Channel MOSFET Driver	1.5A Peak Output Current, 1GΩ Electrical Isolation, SO-8 Package
LTC2053	Zero Drift Instrumentation Amp	Max Gain Error 0.01%, Input Offset Drift of 50nV/°C, Input Offset Voltage of 10μV

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
1923i LT/TP 0701 1.5K • PRINTED IN USA

Precision, Rail-to-Rail, Zero-Drift Instrumentation Amplifier with Resistor-Programmable Gain

FEATURES

- MS8 Package
- Resistor Programmable Gain
- Rail-to-Rail Output
- Maximum Offset Voltage: 10µV
- Maximum Offset Voltage Drift: 50nV/°C
- Supply Operation: 2.7V to 5V
- Typical Noise: $2.5\mu V_{p-p}$ (0.01Hz to 10Hz)
- Typical Supply Current: 0.8mA

APPLICATIONS

- TEC Controllers

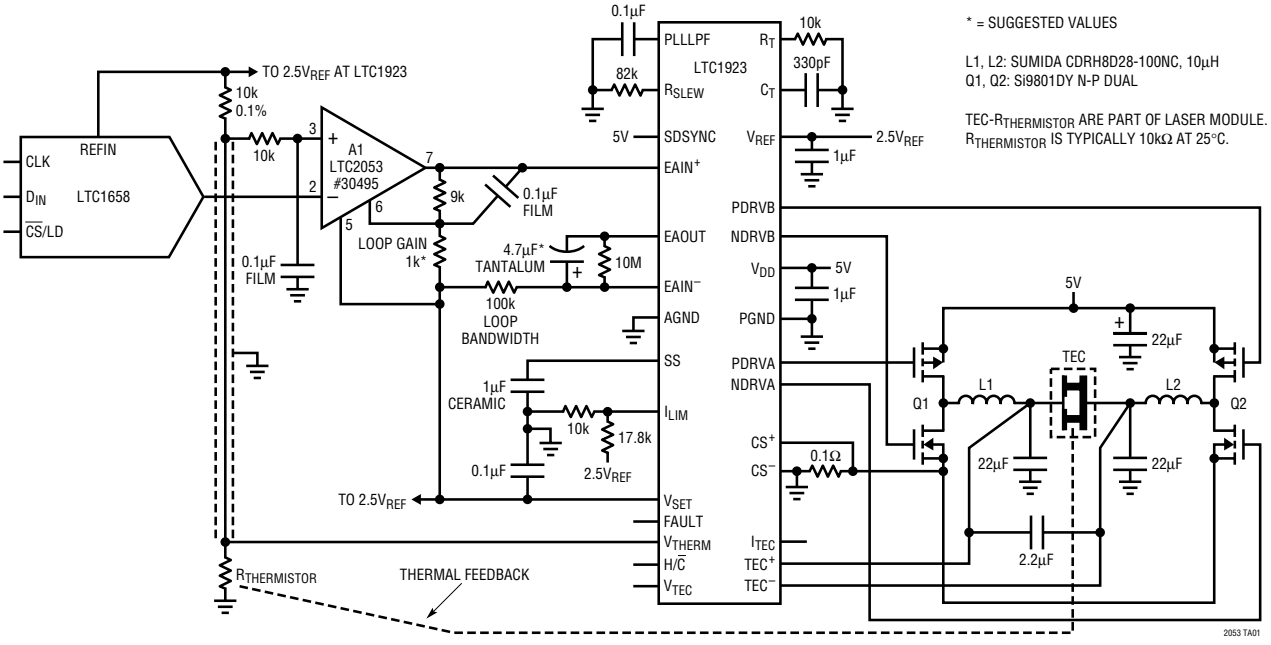
DESCRIPTION

The LTC®2053 SL30495 is a high precision instrumentation amplifier. It uses a charge balanced switched capacitor technique to convert a differential input voltage into a single ended signal that is in turn amplified by a zero-drift operational amplifier. The LTC2053 SL30495 is easy to use; the gain is adjustable with two external resistors, like a traditional op amp.

The single-ended output swings from rail-to-rail. The LTC2053 SL30495 is used in 5V single supply applications.

TYPICAL APPLICATION

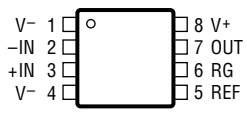
Detailed Schematic of TEC Temperature Controller Includes A1 Thermistor Bridge Amplifier, LTC1923 Switched Mode Controller and Power Output H-Bridge. DAC Establishes Temperature Setpoint. Gain Adjust and Compensation Capacitor Optimize Loop Gain Bandwidth. Various LTC1923 Outputs Permit Monitoring TEC Operating Conditions



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 6V
Input Current ..... ±10mA
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 110°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC2053CMS8#30495
MS8 PART MARKING
LTMW

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 5V, V^- = 0V, REF = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	A_V = 1	●		0.001	0.01	%
Gain Nonlinearity	A_V = 1	●		3	10	ppm
Input Offset Voltage	V_{CM} = 2.5V (Note 1)				10	µV
Average Input Offset Drift	(Note 1)	●			±50	nV/°C
Input Bias Current	V_{CM} = 1V	●		4		nA
Input Offset Current	V_{CM} = 1V	●		1		nA
Input Noise Voltage	DC to 10Hz			2.5		μV_{P-P}
Output Voltage Swing High	R_L = 2k to V^- R_L = 10k to V^-	● ●	4.85 4.95	4.94 4.98		V V
Output Voltage Swing Low					20	mV
Supply Current	No Load	●		0.85	1.2	mA
Internal Sampling Frequency				2.5		kHz

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude the measurements of these voltage levels during automated testing.

PIN FUNCTIONS

V^- (Pins 1, 4): Negative Supply. Both pins must be connected to the negative supply for proper device operation.

–IN (Pin 2): Inverting Input.

+IN (Pin 3): Noninverting Input.

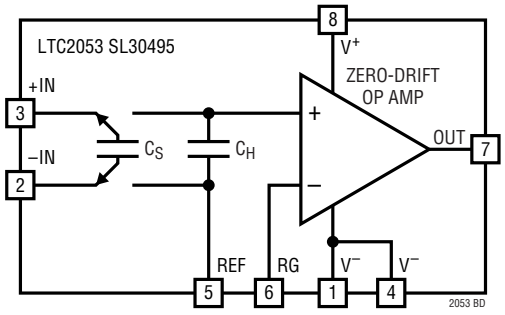
REF (Pin 5): Ground Reference for Output.

RG (Pin 6): Inverting Input of Internal Op Amp. With a resistor, R2, connected between the OUT pin and the RG pin and a resistor, R1, between the RG pin and the REF pin, the DC gain is given by 1 + R2 / R1.

OUT (Pin 7): Amplifier Output.

V^+ (Pin 8): Positive Supply.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Theory of Operation

The LTC2053 SL30495 uses an internal capacitor (C_S) to sample a differential input signal riding on a DC common mode voltage (see Block Diagram). This capacitor's charge is transferred to a second internal hold capacitor (C_H) translating the common mode of the input differential signal to that of the REF pin. The resulting signal is amplified by a zero-drift op amp in the noninverting configuration. The RG pin is the negative input of this op amp and allows external programmability of the DC gain. Simple filtering can be realized by using an external capacitor across the feedback resistor.

Settling Time

The sampling rate is 2.5kHz and the input sampling period during which C_S is charged to the input differential voltage V_{IN} is approximately 180µs. First assume that on each input sampling period, C_S is charged fully to V_{IN}. Since $C_S = C_H$ (=1000pF), a change in the input will settle to N bits of accuracy at the op amp noninverting input after N clock cycles or 400µs(N). The settling time at the OUT pin is also affected by the settling of the internal op amp. Since the gain bandwidth of the internal op amp is typically 200kHz, its settling time alone to N bits would be approximately 0.5µs • N • A_{CL}; where A_{CL} is the closed-loop gain of the op amp. For gains below 100, the settling time is dominated by the switched capacitor front end.

If the input source resistance between +IN and –IN (R_S) is large, C_S may not reach V_{IN} during each input sampling period. The voltage across C_H and C_S will eventually reach V_{IN} but the settling time would be larger than described above. If R_S is less than 20kΩ, then the approximation described above is accurate.

Input Current

Whenever the differential input V_{IN} changes, C_H must be charged up to the new input voltage via C_S. This results in an input charging current during each input sampling period. Eventually, C_H and C_S will reach V_{IN} and, ideally, the input current would go to zero for DC inputs.

In reality, there are additional parasitic capacitors which disturb the charge on C_S every cycle even if V_{IN} is a DC voltage. For example, the parasitic bottom plate capacitor on C_S must be charged from the voltage on the REF pin to the voltage on the –IN pin every cycle. The resulting input charging current decays exponentially during each input sampling period with a time constant equal to R_SC_S, where R_S is the source resistance between +IN and –IN. If the voltage disturbance due to these currents settles before the end of the sampling period, there will be no errors due to source resistance or the source resistance mismatch between –IN and +IN. With R_S less than 20kΩ, no DC errors occur due to this input current.

Grounding and Bypassing

The LTC2053 SL30495 uses a sampled data technique and therefore contains some clocked digital circuitry. It is therefore sensitive to supply bypassing. A 0.1µF ceramic capacitor must be connected between Pin 8 (V^+) and Pin 4 (V^-) with leads as short as possible.

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A Thermoelectric Cooler Temperature Controller for Fiber Optic Lasers

Climatic Pampering for Temperamental Lasers

Jim Williams

INTRODUCTION

Continued demands for increased bandwidth have resulted in deployment of fiber optic-based networks. The fiber optic lines, driven by solid state lasers, are capable of very high information density. Highly packed data schemes such as DWDM (dense wavelength division multiplexing) utilize multiple lasers driving a fiber to obtain large multichannel data streams. The narrow channel spacing relies on laser wavelength being controlled within 0.1nm (nanometer). Lasers are capable of this but temperature variation influences operation. Figure 1 shows that laser output peaks sharply vs wavelength, implying that laser wavelength must be controlled well within 0.1nm to maintain performance. Figure 2 plots typical laser wavelength vs temperature. The 0.1nm/°C slope means that although temperature facilitates tuning laser wavelength, it must not vary once the laser has been peaked. Typically, temperature control of 0.1°C is required to maintain laser operation well within 0.1nm.

Temperature Controller Requirements

The temperature controller must meet some unusual requirements. Most notably, because of ambient temperature variation and laser operation uncertainties, the controller must be capable of either sourcing or removing heat to maintain control. Peltier-based thermoelectric coolers (TEC) permit this but the controller must be truly bidirectional. Its heat flow control must not have dead zone or untoward dynamics in the "hot-to-cold" transition region. Additionally, the temperature controller must be a precision device capable of maintaining control well inside 0.1°C over time and temperature variations.

Laser based systems packaging is compact, necessitating small solution size with efficient operation to avoid excessive heat dissipation. Finally, the controller must operate from a single, low voltage source and its (presumably switched mode) operation must not corrupt the supply with noise.

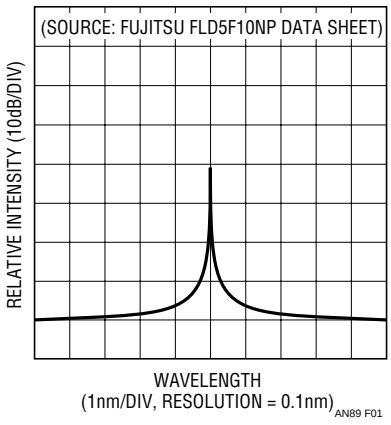

Figure 1. Laser Intensity Peak Approaches 40dB within a 1nm Window

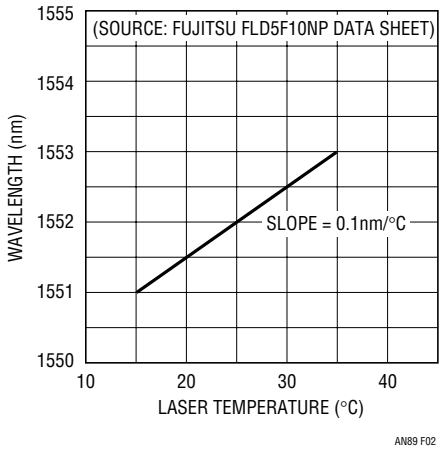

Figure 2. Laser Wavelength Varies ≈0.1nm/°C. Typical Application Requires Wavelength Stability within 0.1nm, Mandating Temperature Control

Temperature Controller Details

Figure 3, a schematic of the thermoelectric cooler (TEC) temperature controller, includes three basic sections. The DAC and the thermistor form a bridge, the output of which is amplified by A1. The LTC1923 controller is a pulse width modulator which provides appropriately modulated and phased drive to the power output stage. The laser is an electrically delicate and very expensive load. As such, the controller provides a variety of monitoring, limiting and overload protection capabilities. These include soft-start and overcurrent protection, TEC voltage and current sense and "out-of-bounds" temperature sensing. Aberrant operation results in circuit shutdown, preventing laser module damage. Two other features promote system level compatibility. A phase-locked loop based oscillator permits reliable clock synchronization of multiple LTC1923s in multilaser systems. Finally, the switched mode power delivery to the TEC is efficient but special considerations are required to ensure that switching related noise is not introduced ("reflected") into the host power supply. The LTC1923 includes edge slew limiting which minimizes switching related harmonics by slowing down the power stages' transition times. This greatly reduces high frequency harmonic content, preventing excessive switching related noise from corrupting the power supply or the laser.[1] The switched mode power output stage, an "H-bridge" type, permits efficient bidirectional drive to the TEC, allowing either heating or cooling of the laser. The thermistor, TEC and laser, packaged at manufacture within the laser module, are tightly thermally coupled.

The DAC permits adjusting temperature setpoint to any individual laser's optimum operating point, normally specified for each laser. Controller gain and bandwidth adjustments optimize thermal loop response for best temperature stability.

Thermal Loop Considerations

The key to high performance temperature control is matching the controller's gain bandwidth to the thermal feedback path. Theoretically, it is a simple matter to do this using conventional servo-feedback techniques. Practi-

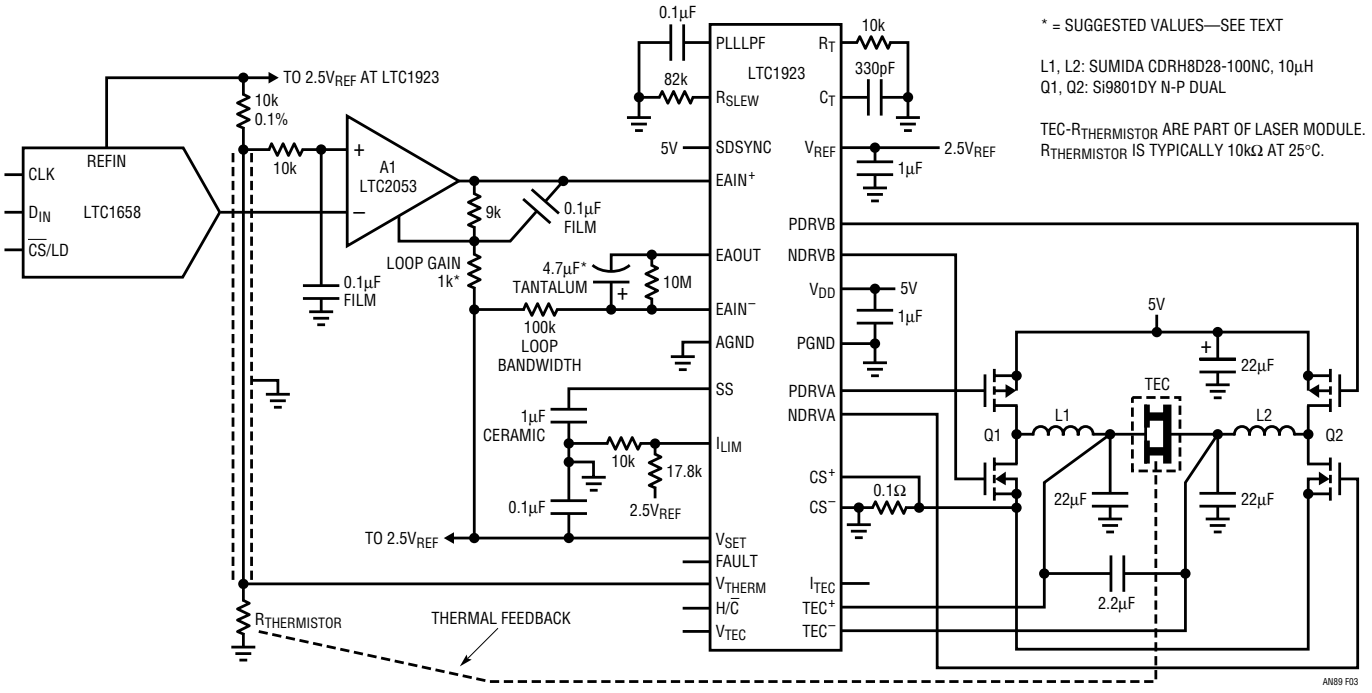

Figure 3. Detailed Schematic of TEC Temperature Controller Includes A1 Thermistor Bridge Amplifier, LTC1923 Switched Mode Controller and Power Output H-Bridge. DAC Establishes Temperature Setpoint. Gain Adjust and Compensation Capacitor Optimize Loop Gain Bandwidth. Various LTC1923 Outputs Permit Monitoring TEC Operating Conditions

Note 1: This technique derives from earlier efforts. See Reference 1 for detailed discussion and related topics.

cally, the long time constants and uncertain delays inherent in thermal systems present a challenge. The unfortunate relationship between servo systems and oscillators is very apparent in thermal control systems.

The thermal control loop can be very simply modeled as a network of resistors and capacitors. The resistors are equivalent to the thermal resistance and the capacitors to thermal capacity. In Figure 4 the TEC, TEC-sensor interface and sensor all have RC factors that contribute to a lumped delay in the system's ability to respond. To prevent oscillation, gain bandwidth must be limited to account for this delay. Since high gain bandwidth is desirable for good control, the delays should be minimized. This is presumably addressed by the laser module's purveyor at manufacture.

The model also includes insulation between the controlled environment and the uncontrolled ambient. The function of insulation is to keep the loss rate down so the temperature control device can keep up with the losses. For any given system, the higher the ratio between the TEC-sensor time constants and the insulation time constants, the better the performance of the control loop.[2]

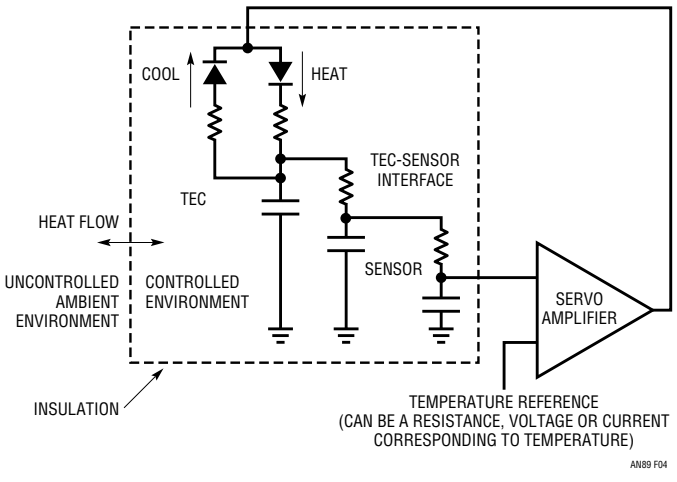

Figure 4. Simplified TEC Control Loop Model Showing Thermal Terms. Resistors and Capacitors Represent Thermal Resistance and Capacity, Respectively. Servo Amplifier Gain Bandwidth Must Accommodate Lumped Delay Presented by Thermal Terms to Avoid Instability

Temperature Control Loop Optimization

Temperature control loop optimization begins with thermal characterization of the laser module. The previous section emphasized the importance of the ratio between the TEC-sensor and insulation time constants. Determination of this information places realistic bounds on achievable controller gain bandwidth. Figure 5 shows results when a typical laser module is subjected to a 40°C step change in ambient temperature. The laser module's internal temperature, monitored by its thermistor, is plotted vs time with the TEC unpowered. An ambient-to-sensor lag measured in minutes shows a classic first order response.

The TEC-sensor lumped delay is characterized by operating the laser module in Figure 3's circuit with gain set at maximum and no compensation capacitor installed. Figure 6 shows large-signal oscillation due to thermal lag dominating the loop. A great deal of valuable information is contained in this presentation.[3] The frequency, primarily determined by TEC-sensor lag, implies limits on how much loop bandwidth is achievable. The high ratio of this frequency to the laser module's thermal time constant (Figure 5) means a simple, dominant pole loop compen-

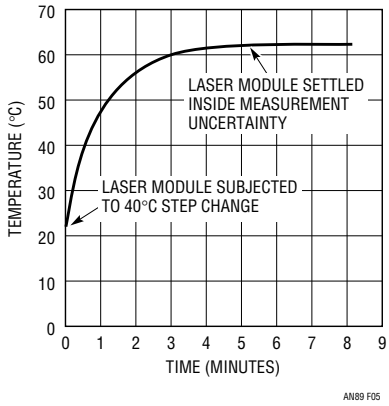

Figure 5. Ambient-to-Sensor Lag Characteristic for a Typical Laser Module Is Set by Package Thermal Resistance and Capacity

Note 2: For the sake of text flow, this somewhat academic discussion must suffer brevity. However, additional thermodynamic gossip appears in Appendix A, "Practical Considerations in Thermoelectric Cooler Based Control Loops."

Note 3: When a circuit "doesn't work" because "it oscillates," whether at millihertz or gigahertz, four burning questions should immediately dominate the pending investigation. What frequency does it oscillate at, what is the amplitude, duty cycle and waveshape? The solution invariably resides in the answers to these queries. Just stare thoughtfully at the waveform and the truth will bloom.

sation will be effective. The saturation limited waveshape suggests excessive gain is driving the loop into full cooling and heating states. Finally, the asymmetric duty cycle reflects the TEC's differing thermal efficiency in the cooling and heating modes.

Controller gain bandwidth reduction from Figure 6's extremes produced Figure 7's display. The waveform results from a small step (≈0.1°C) change in temperature setpoint. Gain bandwidth is still excessively high, producing a damped, ringing response over 2 minutes in duration! The loop is just marginally stable. Figure 8's test conditions are identical but gain bandwidth has been significantly reduced. Response is still not optimal but settling occurs in ≈4.5 seconds, about 25x faster than the previous case. Figure 9's response, taken at further reduced gain bandwidth settings, is nearly critically damped and settles cleanly in about 2 seconds. A laser module optimized in this fashion will easily attenuate external temperature shifts by a factor of thousands without overshoots or excessive lags. Further, although there are substantial thermal differences between various laser modules, some generalized guidelines on gain bandwidth values are possible.[4] A DC gain of 1000 is sufficient for required temperature control, with bandwidth below 1Hz providing adequate loop stability. Figure 3's suggested gain and bandwidth values reflect these conclusions, although stability testing for any specific case is mandatory.

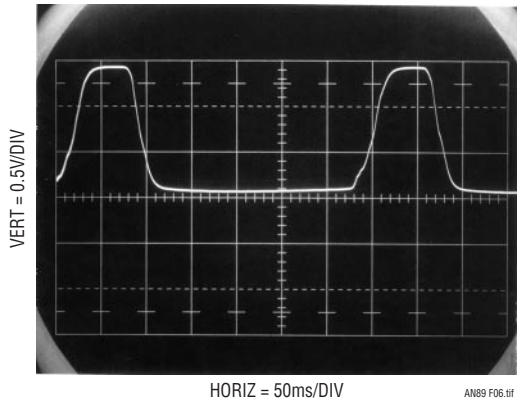

Figure 6. Deliberate Excess of Loop Gain Bandwidth Introduces Large-Signal Oscillation. Oscillation Frequency Provides Guidance for Achievable Closed-Loop Bandwidth. Duty Cycle Reveals Asymmetric Heating-Cooling Mode Gains

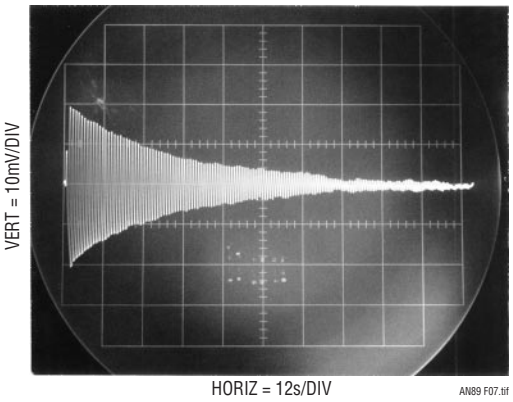

Figure 7. Loop Response to Small Step in Temperature Setpoint. Gain Bandwidth Is Excessively High, Resulting in Damped, Ringing Response Over 2 Minutes in Duration

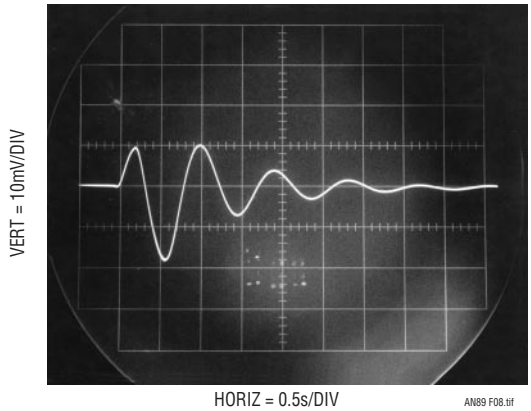

Figure 8. Same Test Conditions as Figure 7 but at Reduced Loop Gain Bandwidth. Loop Response Is Still Not Optimal but Settling Occurs in 4.5 Seconds—Over 25x Faster than Previous Case

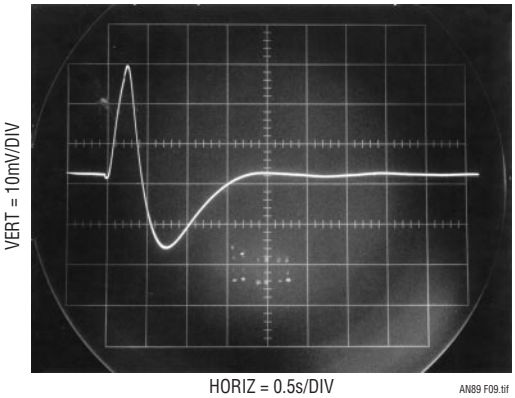

Figure 9. Gain Bandwidth Optimization Results in Nearly Critically Damped Response with Settling in 2 Seconds

Note 4: See Appendix A, "Practical Considerations in Thermoelectric Cooler Based Control Loops," for additional comment.

Temperature Stability Verification

Once the loop has been optimized, temperature stability can be measured. Stability is verified by monitoring thermistor bridge offset with a stable, calibrated differential amplifier.[5] Figure 10 records ±1 millidegree baseline stability over 50 seconds in the cooling mode. A more stringent test measures longer term stability with significant variations in ambient temperature. Figure 11's strip-chart recording measures cooling mode stability against an environment that steps 20°C above ambient every hour over 9 hours.[6] The data shows 0.008°C resulting variation, indicating a thermal gain of 2500.[7] The 0.0025°C baseline tilt over the 9 hour plot length derives from varying ambient temperature. Figure 12 utilizes identical test conditions, except that the controller operates in the heating mode. The TEC's higher heating mode efficiency furnishes greater thermal gain, resulting in a 4x stability improvement to about 0.002°C variation. Baseline tilt, just detectable, shows a similar 4x improvement vs Figure 11.

This level of performance ensures the desired stable laser characteristics. Long-term (years) temperature stability is primarily determined by thermistor aging characteristics.[8]

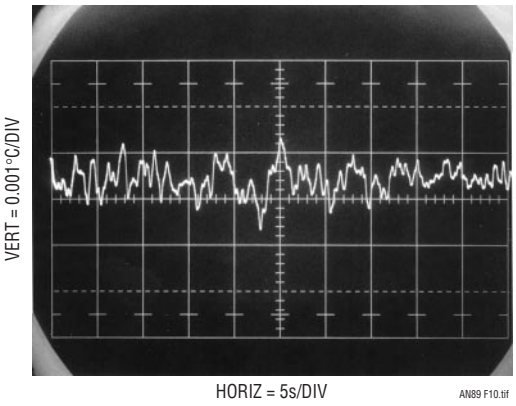

Figure 10. Short-Term Monitoring in Room Environment Indicates 0.001°C Cooling Mode Baseline Stability

Note 5: This measurement monitors thermistor stability. Laser temperature stability will be somewhat different due to slight thermal decoupling and variations in laser power dissipation. See Appendix A.

Note 6: That's right, a *strip-chart recording*. Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be a factor.

Note 7: Thermal gain is temperature control aficionado jargon for the ratio of ambient-to-controlled temperature variation.

Note 8: See Appendix A for additional information.

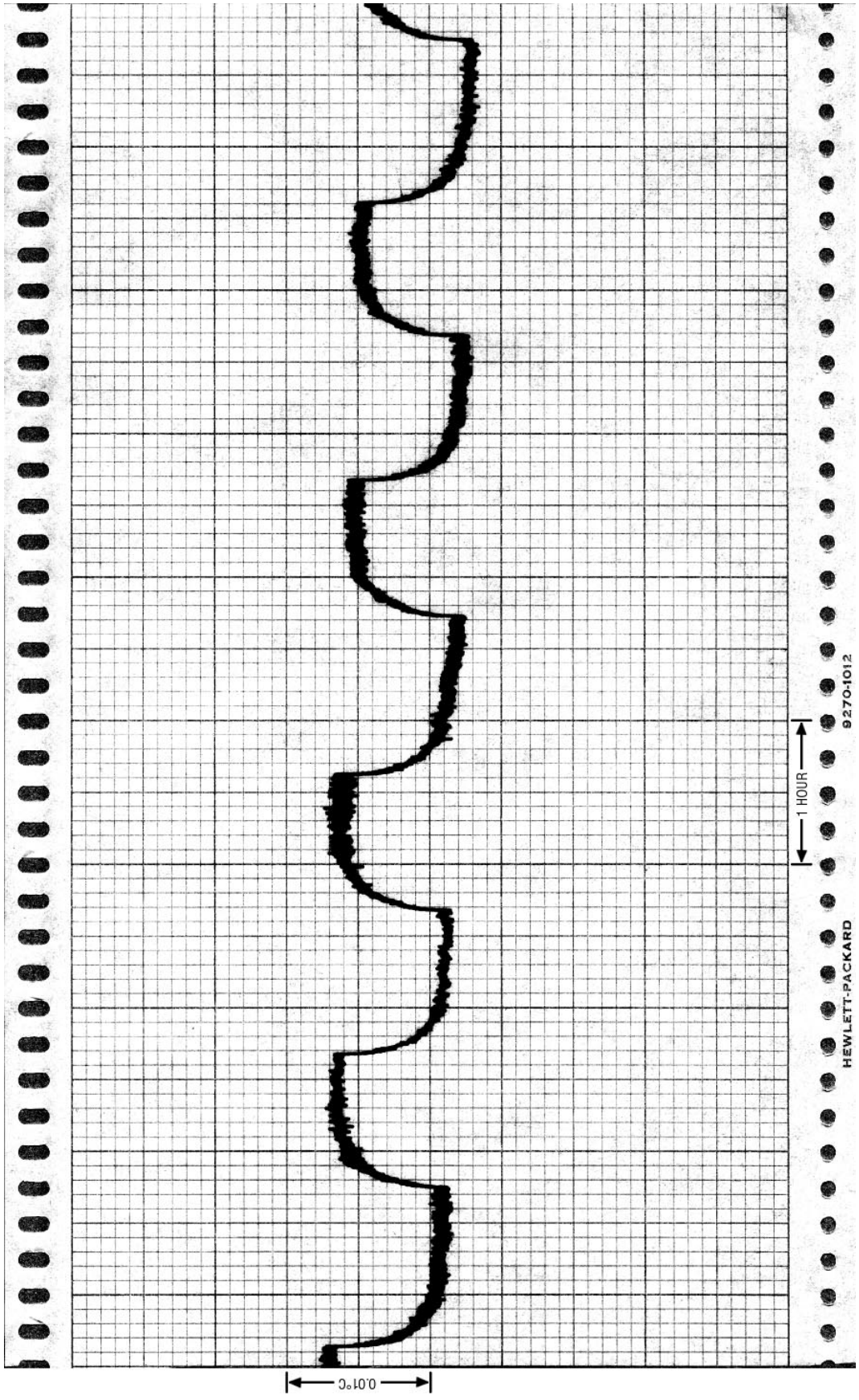

Figure 11. Long-Term Cooling Mode Stability Measured in Environment that Steps 20 Degrees Above Ambient Every Hour. Data Shows Resulting 0.008°C Peak-to-Peak Variation, Indicating Thermal Gain of 2500. 0.0025°C Baseline Tilt Over Plot Length Derives From Varying Ambient Temperature

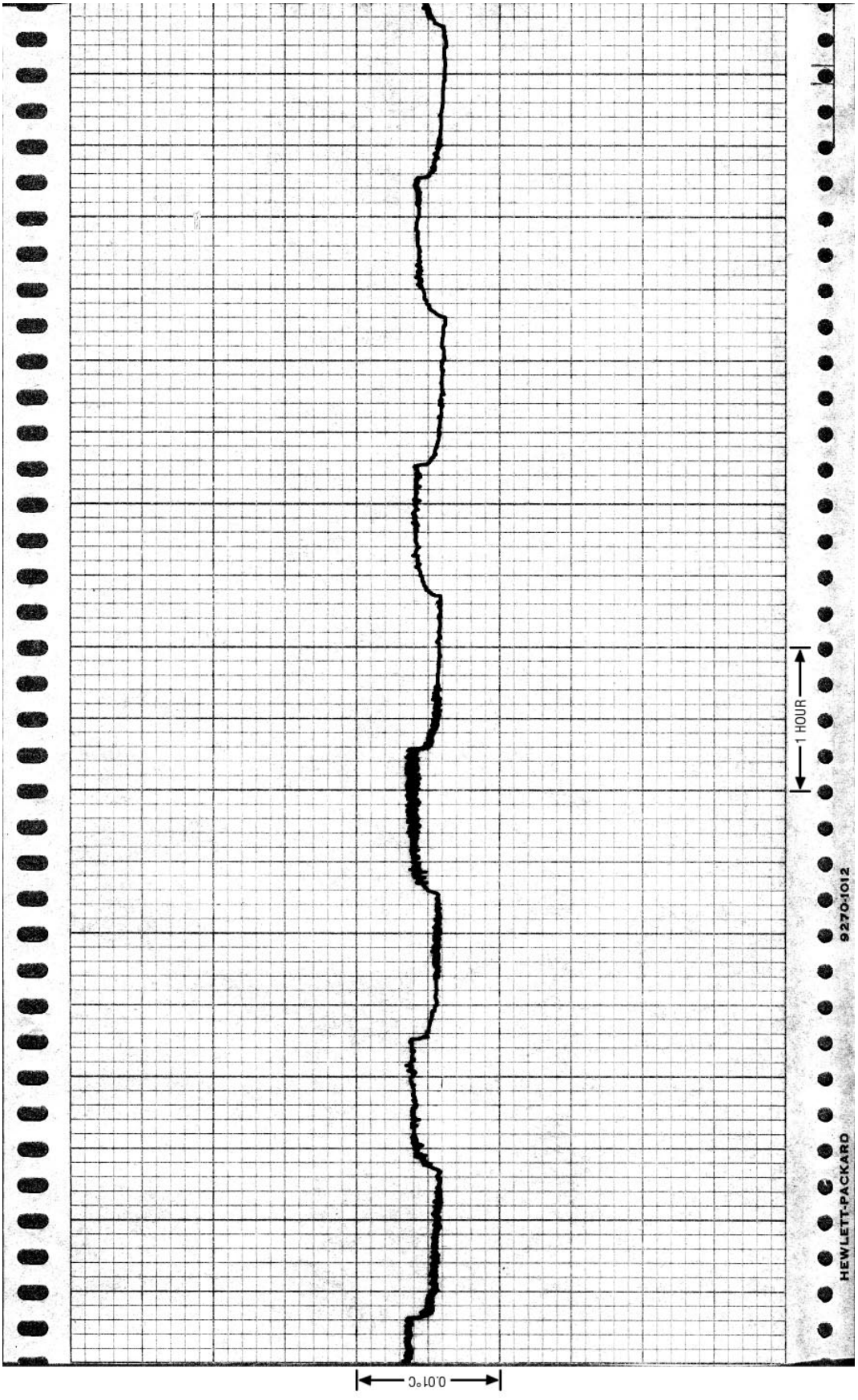

Figure 12. Identical Test Conditions as Figure 11, Except in Heating Mode. TEC's Higher Heating Mode Efficiency Results in Higher Thermal Gain. 0.002°C Peak-to-Peak Variation Is 4x Stability Improvement. Baseline Tilt, Just Detectable, Shows Similar 4x Improvement vs Figure 11

Reflected Noise Performance

The switched mode power delivery to the TEC provides efficient operation but raises concerns about noise injected back into the host system via the power supply. In particular, the switching edge's high frequency harmonic content can corrupt the power supply, causing system level problems. Such "reflected" noise can be troublesome to deal with. The LTC1923 avoids these issues by controlling the slew of its switching edges, minimizing high frequency harmonic content.[9] This slowing down of switching transients typically reduces efficiency by only 1% to 2%, a small penalty for the greatly improved noise performance. Figure 13 shows noise and ripple at the 5V supply with slew control in use. Low frequency ripple, 12mV in amplitude, is usually not a concern, as opposed to the high frequency transition related-components, which are much lower. Figure 14, a time and amplitude expansion of Figure 13, more clearly studies high frequency residue. High frequency amplitude, measured at center screen, is about 1mV. The slew limiting's effectiveness is measured in Figure 15 by disabling it. High frequency content jumps to nearly 10mV, almost 10x worse performance. Leave that slew limiting in there!

Most applications are well served by this level of noise reduction. Some special cases may require even lower reflected noise. Figure 16's simple LC filter may be employed in these cases. Combined with the LTC1923's slew limiting, it provides vanishingly small reflected ripple and

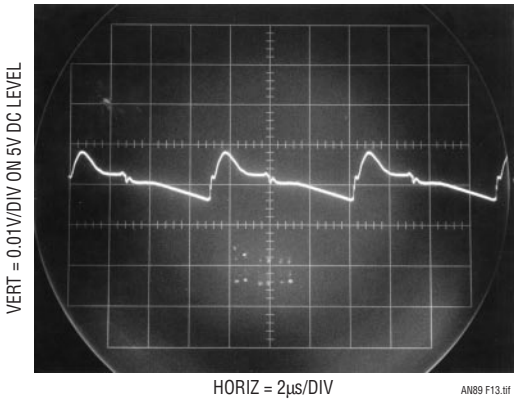

Figure 13. "Reflected" Noise at 5VDC Input Supply Due to Switching Regulator Operation with Edge Slew Rate Limiting in Use. Ripple Is 12mV$_{P-P}$, High Frequency Edge Related Harmonic Is Much Lower

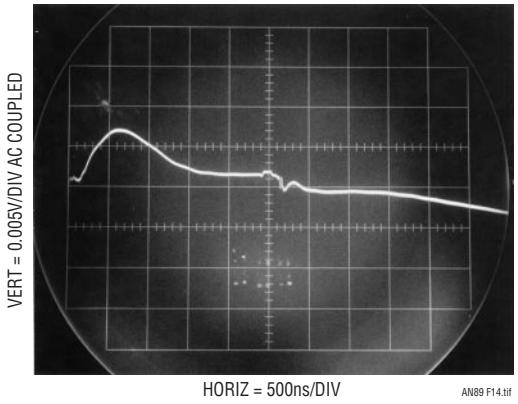

Figure 14. Time and Amplitude Expansion of Figure 13 More Clearly Shows Residual High Frequency Content with Slew Limiting Employed

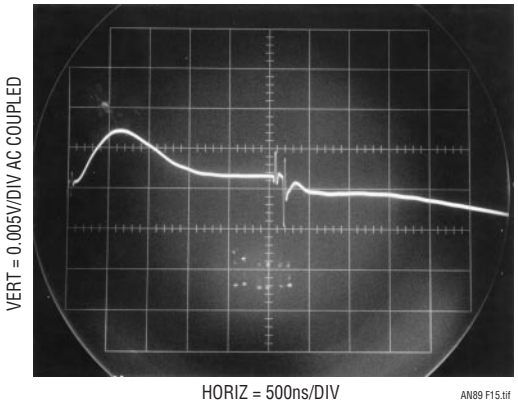

Figure 15. Same Test Conditions as Previous Figure, Except Slew Limiting Is Disabled. High Frequency Harmonic Content Rises ≈x10. Leave that Slew Limiting in There!

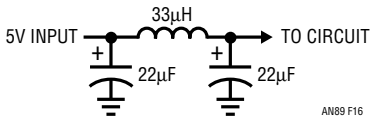

Figure 16. LC Filter Produces 1mV Reflected Ripple and 500µV High Frequency Harmonic Noise Residue

Note 9: This technique derives from previous work. See Reference 1.

high frequency harmonics. Figure 17, taken using this filter, shows only about 1mV of ripple, with submillivolt levels of high frequency content. Figure 18 expands the time scale to examine the high frequency remnants. Amplitude is 500μV, about 1/3 Figure 14's reading. As before, slew limiting effectiveness is measurable by disabling it. This is done in Figure 19, with a resulting 4.4x increase in high frequency content to about 2.2mV. As in Figure 15, if lowest reflected noise is required, leave that slew limiting in there!

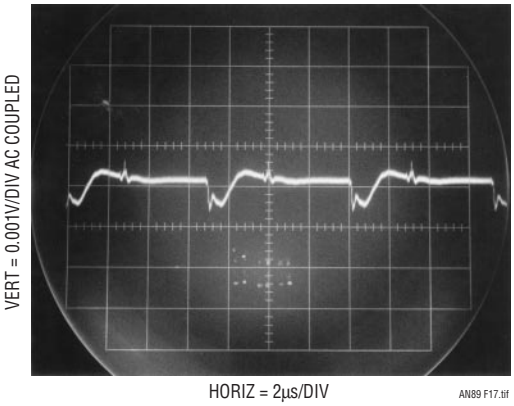

Figure 17. 5V Supply Reflected Ripple Measures 1mV with Figure 16's LC Filter in Use, a 10x Reduction Over Figure 13. Switching Edge Related Harmonic Content Is Small Due to Slew Limiting Action

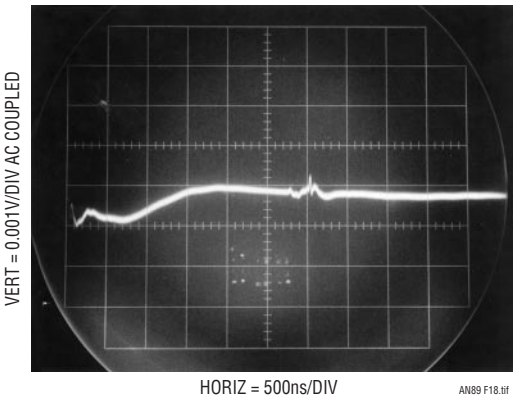

Figure 18. Horizontal Expansion Permits Study of High Frequency Harmonic with Slew Limiting Enabled. Amplitude Is 500μV, About 1/3 Figure 14's Reading

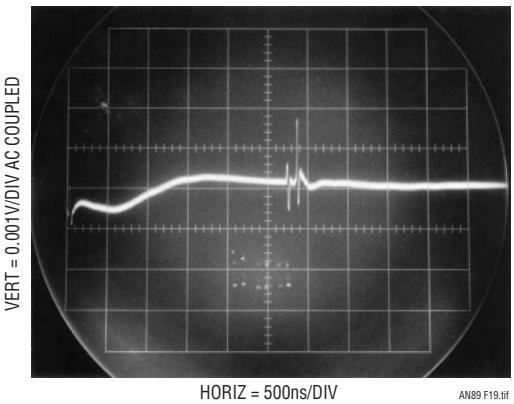

Figure 19. Same Conditions as Previous Figure, Except Slew Limiting Is Disabled. Harmonic Content Amplitude Rises to 2.2mV, a 4.4x Degradation. As in Figure 15, Leave that Slew Limiting in There!

REFERENCES

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7. Williams, J., "Designer's Guide to Temperature Control," *EDN* Magazine, June 20, 1977.
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Note: This Application Note was derived from a manuscript originally prepared for publication in EDN magazine.

APPENDIX A

PRACTICAL CONSIDERATIONS IN THERMOELECTRIC COOLER BASED CONTROL LOOPS

There are a number of practical issues involved in implementing thermoelectric cooler (TEC) based control loops. They fall within three loosely defined categories. These include temperature setpoint, loop compensation and loop gain. Brief commentary on each category is provided below.

Temperature Setpoint

It is important to differentiate between temperature accuracy and stability requirements. The exact temperature setpoint is not really important, so long as it is stable. Each individual laser's output maximizes at some temperature (see text Figures 1 and 2). Temperature setpoint is typically incremented until this peak is achieved. After this, only temperature setpoint stability is required. This is why thermistor tolerances on laser module data sheets are relatively loose (5%). Long-term (years) temperature setpoint stability is primarily determined by thermistor stability over time. Thermistor time stability is a function of operating temperatures, temperature cycling, moisture contamination and packaging. The laser modules' relatively mild operating conditions are very benign, promoting good long-term stability. Typically, assuming good grade thermistors are used at module fabrication, thermistor stability comfortably inside 0.1°C over years may be expected.

Also related to temperature setpoint is that the servo loop controls *sensor* temperature. The laser operates at a somewhat different temperature, although laser temperature stability depends upon the stable loop controlled environment. The assumption is that laser dissipation constant remains fixed, which is largely true.[1]

Loop Compensation

Figure 3's "dominant pole" compensation scheme takes advantage of the long time constant from ambient into the laser module (see text Figure 5). Loop gain is rolled off at a frequency low enough to accommodate the TEC-thermistor lag (see text Figure 6) but high enough to smooth transients arriving from the outside ambient. The relatively high TEC-thermistor to module insulation time constant ratio (<1 second to minutes) makes this approach viable. Attempts at improving loop response with more sophisticated compensation schemes encounter difficulty due to laser module thermal term uncertainties. Thermal terms can vary significantly between laser module brands,

Note 1: Academics will be quick to note that this phenomenon also occurs in the sensor's operation. Strictly speaking, the sensor operates at a slightly elevated temperature from its nominally isothermal environment. The assumption is that its dissipation constant remains fixed, which is essentially the case. Because of this, its temperature is stable.

rendering tailored compensation schemes impractical or even deleterious. Note that this restriction still applies, although less severely, even for modules of "identical" manufacture. It is very difficult to maintain tight thermal term tolerances in production.

The simple dominant pole compensation scheme provides good loop response over a wide range of laser module types. It's the way to go.

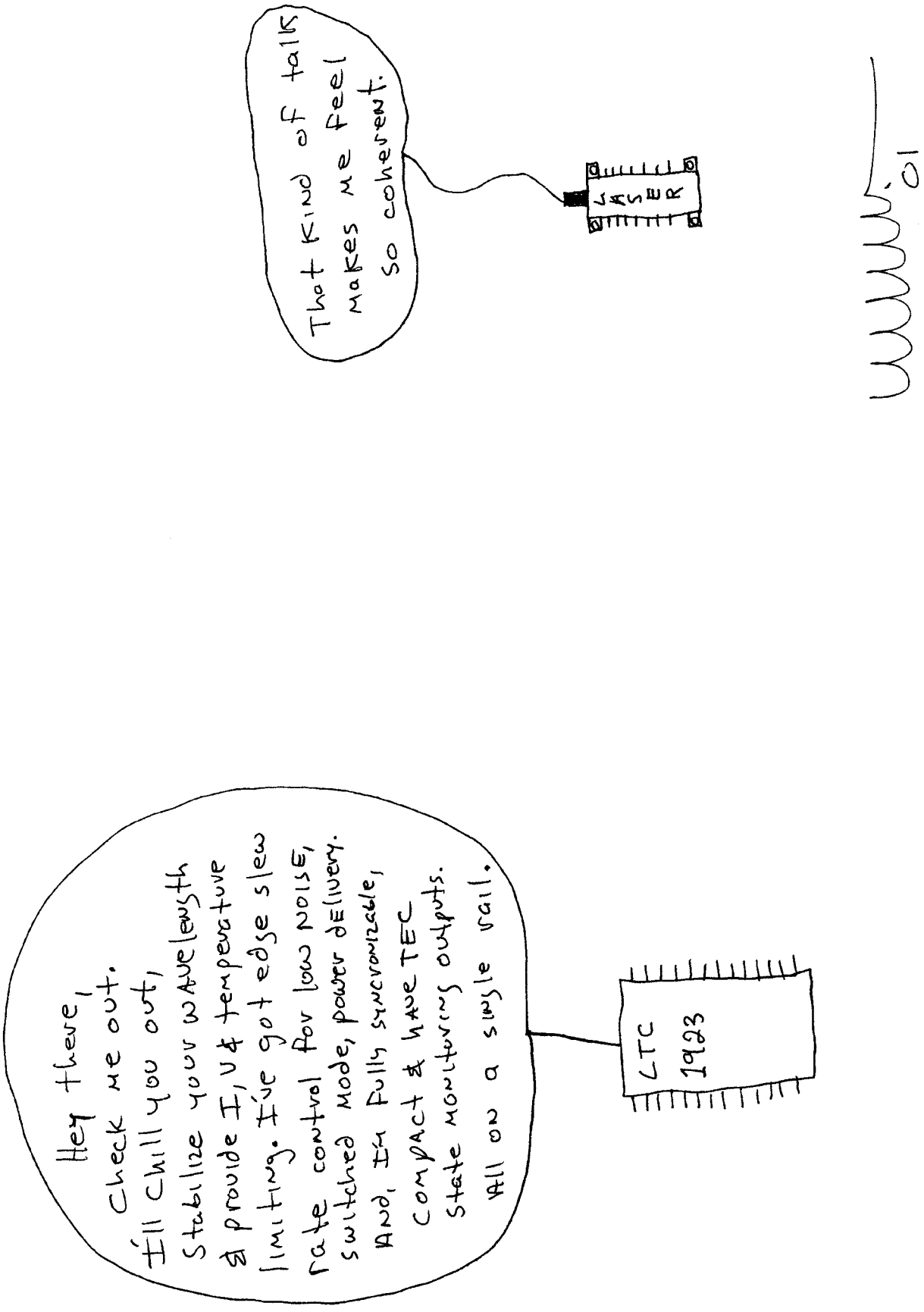
Loop Gain

Loop gain is set by both electrical and thermal gain terms. The most unusual aspect of this is different TEC gain in heating and cooling modes. Significantly more gain is available in heating mode, accounting for the higher stabilities noted in the text (Figures 11 and 12). This higher gain means that loop gain bandwidth limits should be determined in heating mode to avoid unpleasant surprises. Figure 3's suggested loop gain and compensation values reflect this. It is certainly possible to get cute by changing loop gain bandwidth with mode but performance improvement is probably not worth the ruckus.[2]

It is important to remember that the TEC is a heat pump, the efficiency of which depends on the temperature across it. Gain varies with efficiency, degrading temperature stability as efficiency decreases. The laser module should be well coupled to some form of heat sink.[3] The small amount of power involved does not require large sink capability but adequate thermal flow must be maintained. Usually, coupling the module to the circuit's copper ground plane is sufficient, assuming the plane is not already thermally biased.

Note 2: The LTC1923's "heat-cool" status pin beckons alluringly.

Note 3: Yes, this means you should use that messy white goop. A less obnoxious alternative is the thermally conductive gaskets, which are nearly as good.



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1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com

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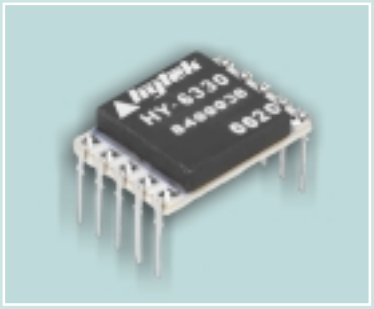
Switchable Constant Current Laser Diode Driver



Features:

- Adjustable current to 170mA @ 5Volts
- Enable/disable pin
- For common cathode or isolated laser diode current drive
- Very small size
- Thru-hole or surface-mount package option

Description:

The HY6330 Laser Diode Driver is a programmable voltage controlled constant current transconductance amplifier with optical feedback.

The HY6330 is used in applications that require a stable, selectable current source to drive a laser diode. The current is selectable from zero to over 170mA. Constant optical output power can be maintained using feedback from a back facet photodetector. Optical output can also be monitored using the voltage proportional output provided. The HY6330 comes in 10-pin thruhole or surface mount packages.

The HY6330 is designed for applications requiring constant current drive for the operation of laser diodes such as pump sources for EDFA's telecom lasers, and diode pumped semiconductors.

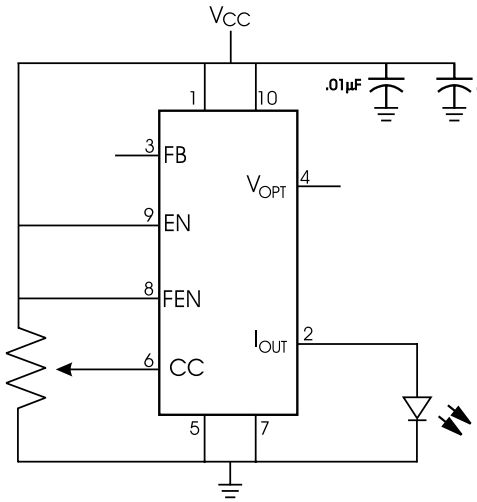


FIGURE 1

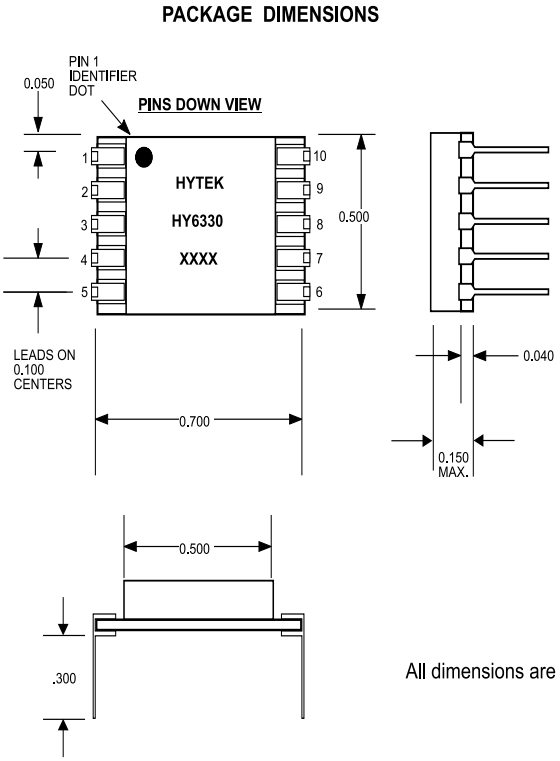


FIGURE 2

Input Specifications

Power Supply Input (V_{CC}): **Pins 1, 10**	+5 to +8V @250mA max.
Drive Enable (EN): **Pin 9**	GND (off, disable), V_{CC} or open (on, enable)
Current Control (CC): **Pin 6**	0 to 200mA for input voltage 0 to V_{CC}
Ground (GND): **Pins 5, 7**	Power supply ground
Feedback-Optical (FB): **Pin 3**	0 <FB <V_{CC}
Feedback-Enable (FEN): **Pin 8**	V_{CC} (disable), GND or open (enable)

Output Specifications

Laser Diode Current Drive (I_{OUT}): **Pin 2**	0 to 170mA @ 5V, 0 to 250mA @ 8V
Optical Output Monitor (V_{OPT}): Pin 4	Range 0–4V

Environmental Conditions

Operating Temperature	–20°C to 100°C (case)
Storage Temperature	–65°C to 150°C (case)

Signal Descriptions

V_{CC} Input power supply, +5 Volts typical

EN The Enable pin is used to enable/disable the output. When the Enable pin is connected to ground, the output is disabled. When this pin is connected to V_{CC} or left open, the laser current is enabled, allowing current to flow through the laser diode.

CC The current is set by the voltage at the current control input. The voltage, on the current control input, programs the laser diode drive current, I_{OUT}. When the input is at GND the modulation current is zero. Maximum laser current occurs when this voltage is V_{CC}.

GND Ground return for V_{CC} (input power supply).

FB This high impedance input is used with a photodetector to control Output Current.

FEN At V_{CC} this input disables Feedback on Pin 3, which allows diode current to be set by Pin 6.

I_{OUT} This Output provides drive current to the laser diode; (anode/positive; connect cathode to ground). Maximum drive current is dependent upon laser diode impedance and power supply input voltage.

V_{OPT} The optical monitor voltage is proportional to the optical output power of the laser diode as sensed by a backfacet photodetector over the range of 1µA to 1mA.

19-1098; Rev 1; 12/96

MAXIM

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX525 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX525 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated via the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

- ♦ **Four 12-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation**
  10µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **Capable of Recalling Last State Prior to Shutdown**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**

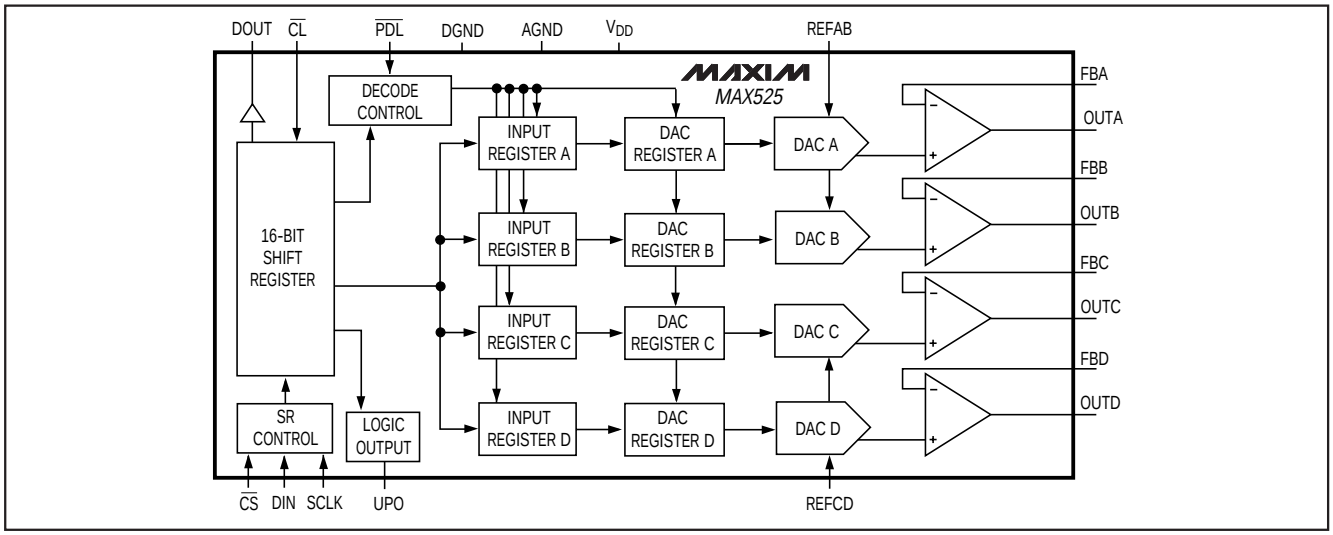
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX525ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX525BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX525ACAP	0°C to +70°C	20 SSOP	±1/2
MAX525BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW

Operating Temperature Ranges
MAX525_C_P .....0°C to +70°C
MAX525_E_P .....-40°C to +85°C
MAX525_MJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX525A		±0.25	±0.5	LSB
		MAX525B			±1.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE			-0.8	±2.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		100	600	µV/V
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE			-0.8	±2.0	LSB
Offset Error				±1.0	±6.0	mV
Integral Nonlinearity	INL			±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555 hex	10			kΩ
Reference Current in Shutdown				0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		12		µs
Output Voltage Swing		Rail to rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				15		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.85	0.98	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Accuracy is better than 1.0LSB for V_{OUT} = 6mV to V_{DD} - 60mV, guaranteed by PSR test on end points.
Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

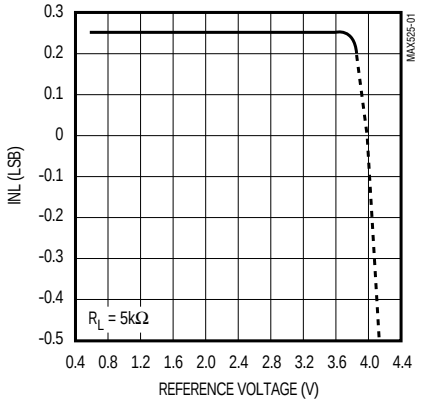
(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

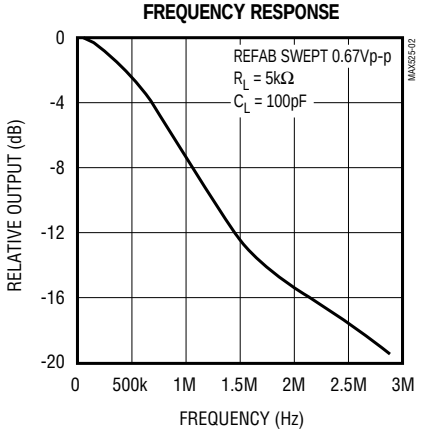
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

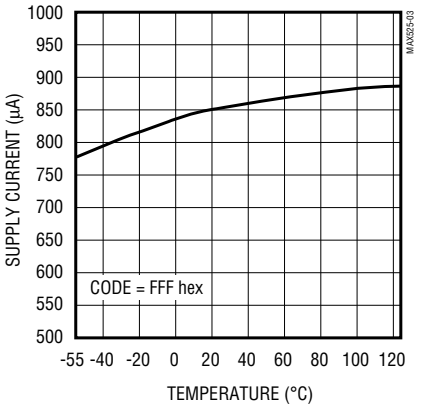
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



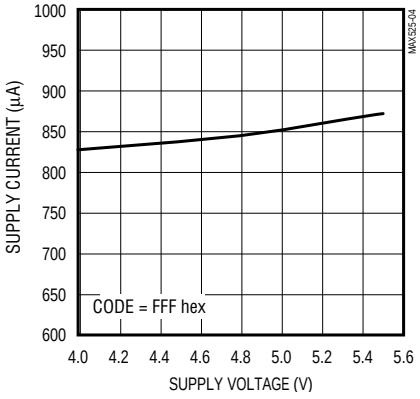
SUPPLY CURRENT vs. TEMPERATURE



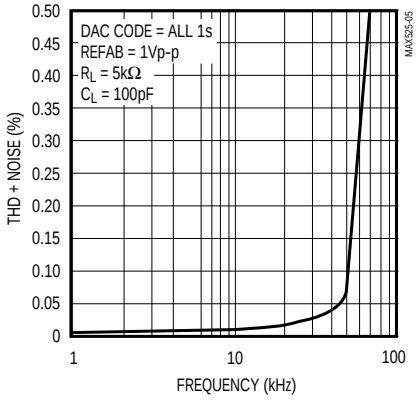
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

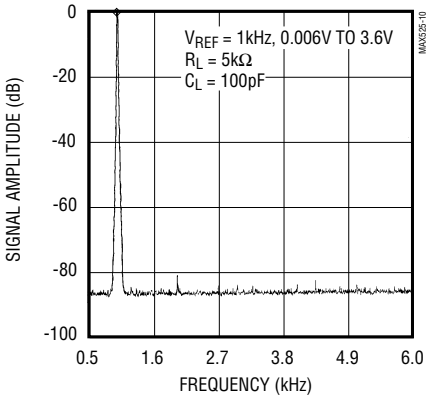
SUPPLY CURRENT vs. SUPPLY VOLTAGE



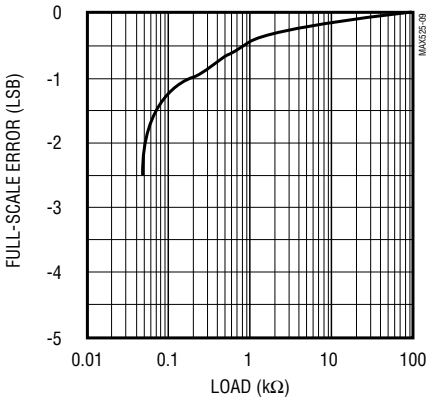
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



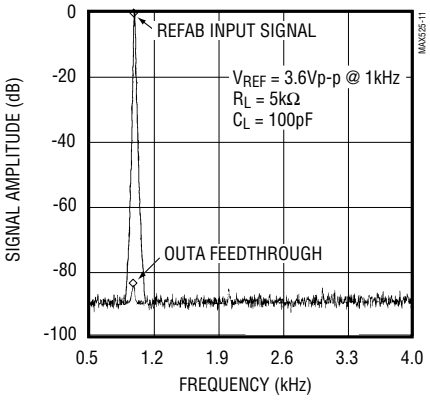
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

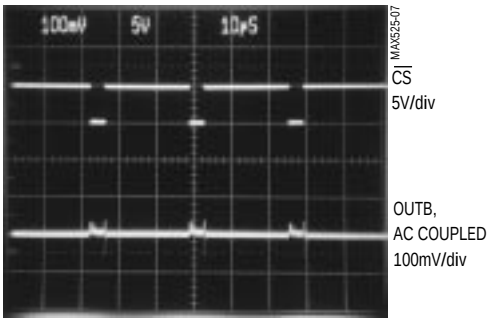


Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

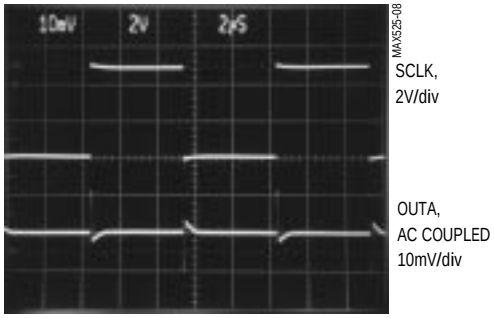
MAJOR-CARRY TRANSITION



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF

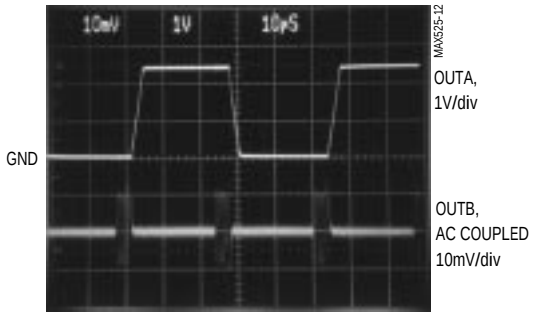
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 5V, DIN = 0V
DAC A CODE SET TO 800 hex

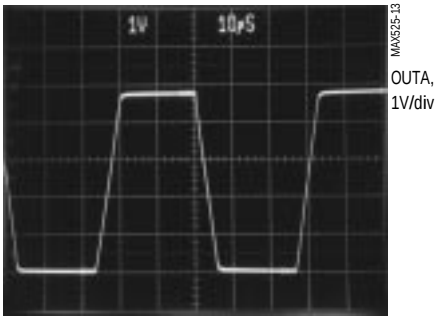
ANALOG CROSSTALK



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
DAC A CODE SWITCHING FROM 00B hex TO FFF hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clear All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

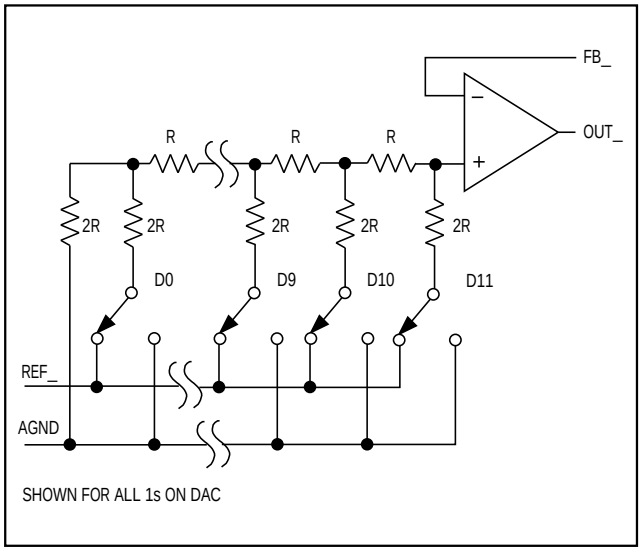


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX525 contains four 12-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 555 hex, to a high value exceeding several gigohms (leakage currents) with an input code of 000 hex. Because the input impedance at the reference pins is code-dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.025LSB (0.061LSB worst case) when driving both MAX525 reference inputs simultaneously at 2.5V. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX525's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All MAX525 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX525 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX525 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Power-Down Mode

The MAX525 features a software-programmable shutdown that reduces supply current to a typical value of 10µA. The power-down lockout ($\overline{PDL}$) pin must be high to enable the shutdown mode. Writing 1100XXXXXXXXXXX as the input-control word puts the MAX525 in power-down mode (Table 1).

In power-down mode, the MAX525 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in power-down, allowing the MAX525 to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 15µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX525's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX525's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX525's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX525's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX525 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 12 data bits D11…D0 (Figure 4). The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when coming out of shutdown mode.

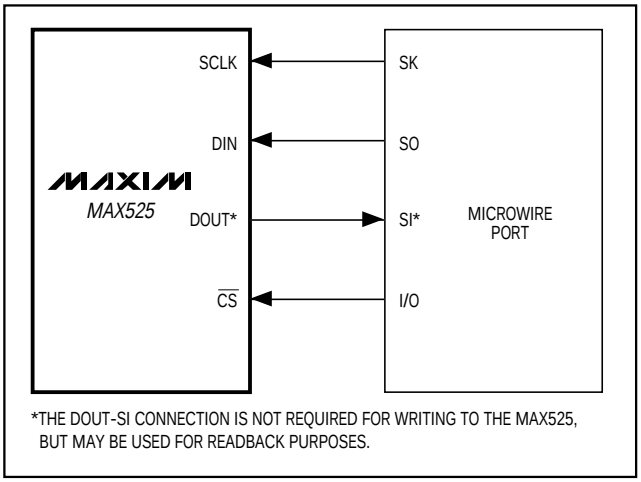


Figure 2. Connections for Microwire

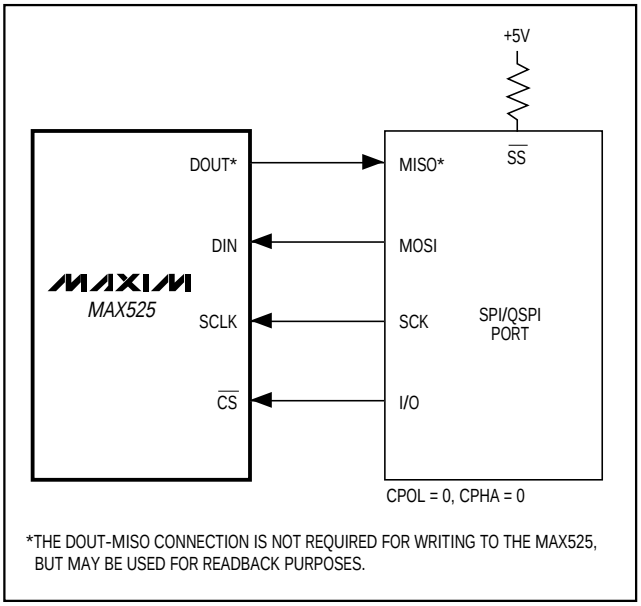


Figure 3. Connections for SPI/QSPI

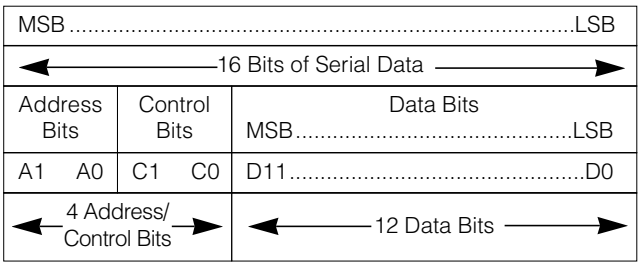


Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.....D0 MSB LSB	
0	0	0	1	12-bit DAC data	Load input register A; DAC registers unchanged.
0	1	0	1	12-bit DAC data	Load input register B; DAC registers unchanged.
1	0	0	1	12-bit DAC data	Load input register C; DAC registers unchanged.
1	1	0	1	12-bit DAC data	Load input register D; DAC registers unchanged.
0	0	1	1	12-bit DAC data	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (start-up).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (start-up).
1	1	0	0	XXXXXXXXXXXX	Shutdown (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX525 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX525 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX525 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire™, SPI™/QSPI™, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX525 serial interface (Table 1).

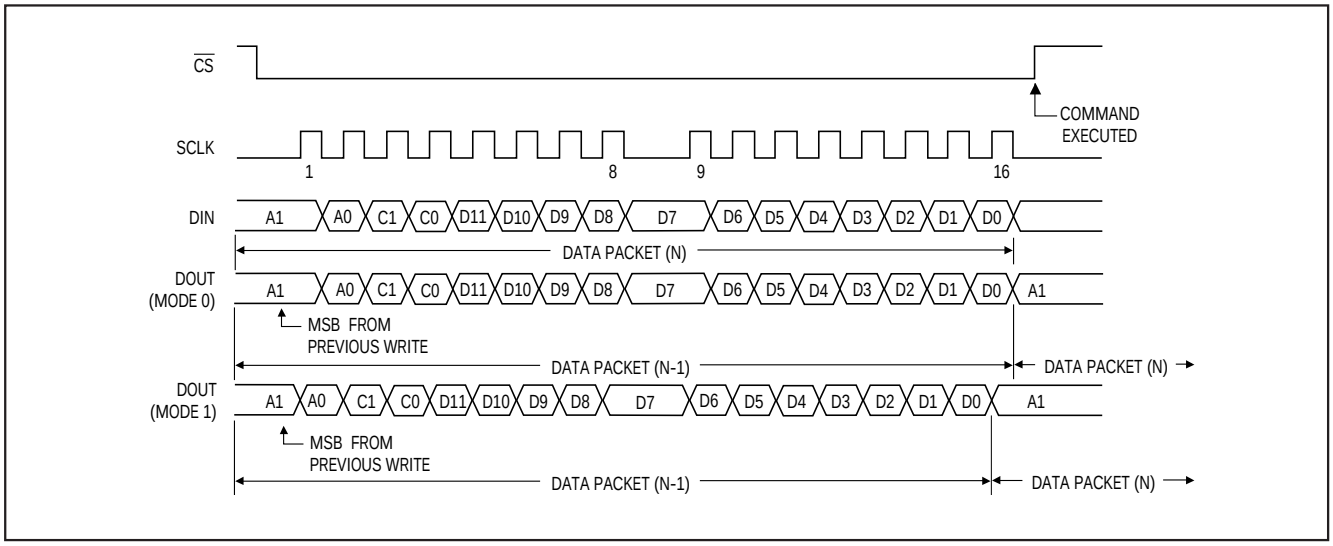


Figure 5. Serial-Interface Timing Diagram

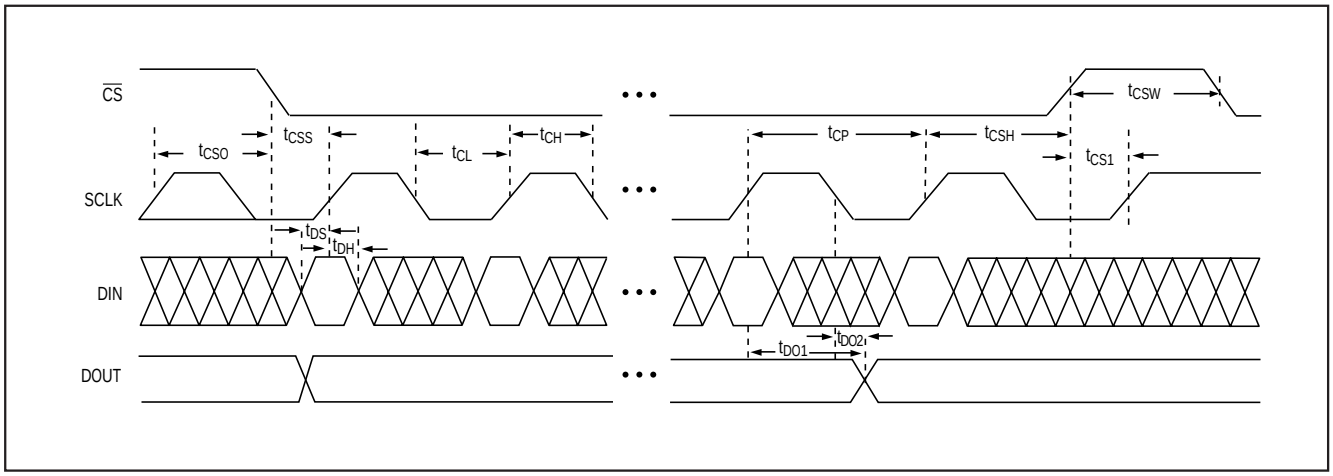


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout (PDL)

The power-down lockout pin PDL disables software shutdown when low. When in shutdown, transitioning PDL from high to low wakes up the part with the output set to the state prior to shutdown. PDL could also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX525s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX525's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX525s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input (CS) is required for each IC.

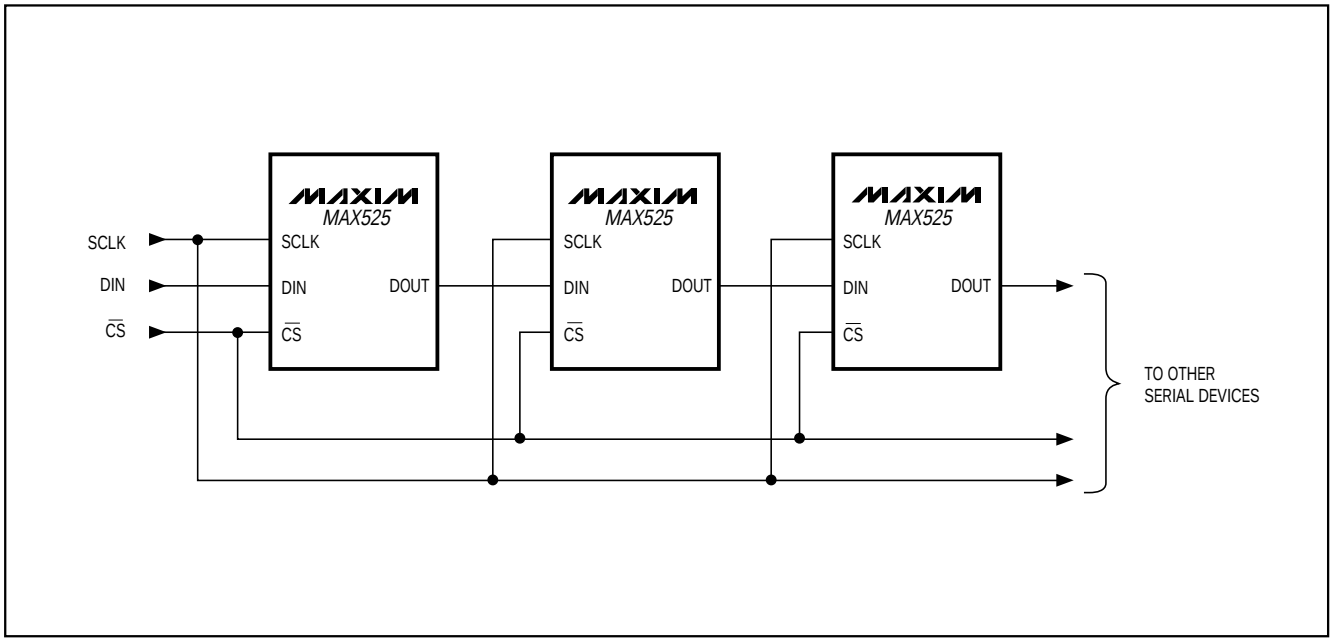


Figure 7. Daisy-Chaining MAX525s

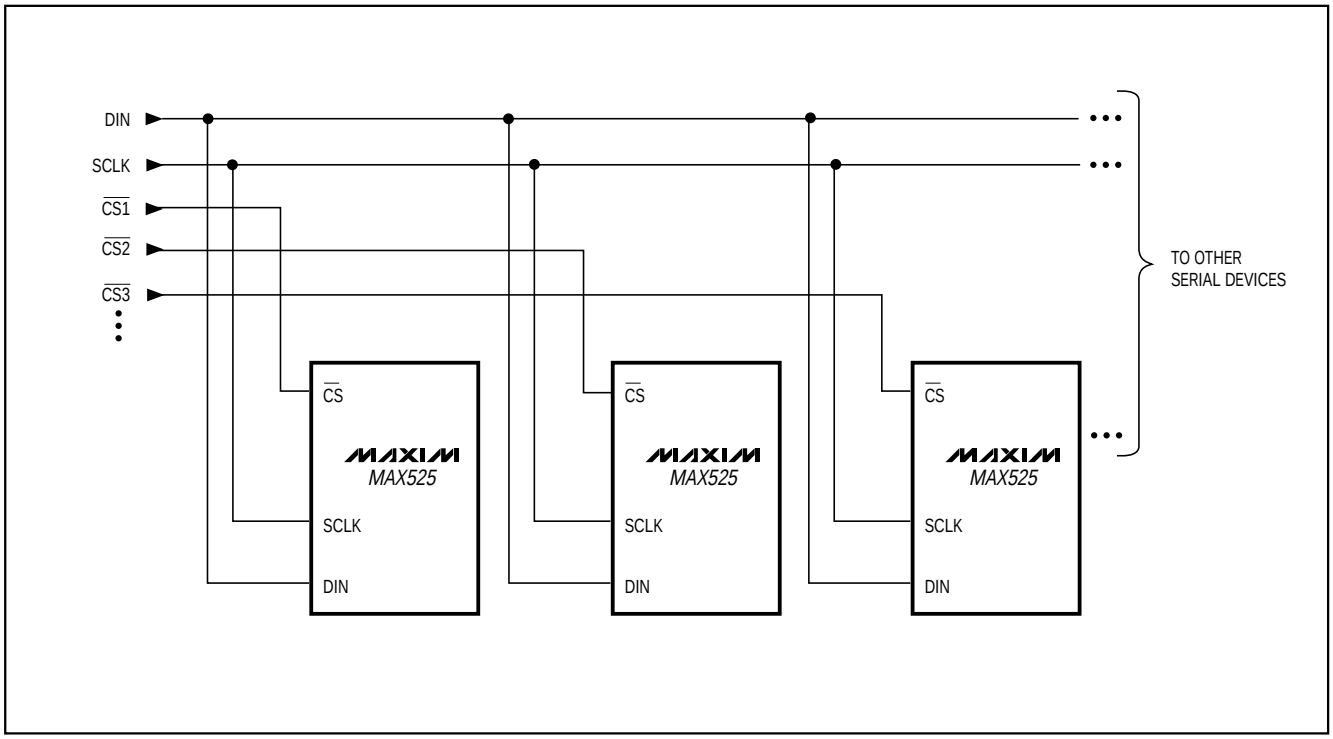


Figure 8. Multiple MAX525s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX525 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX525 with the output amplifiers configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Bipolar Output

The MAX525 outputs can be configured for bipolar operation using Figure 11's circuit.

$$V_{OUT} = V_{REF} [(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$+V_{REF}\left(\frac{2048}{4096}\right) = \frac{+V_{REF}}{2}$
0111 1111 1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

Note: $1LSB = (V_{REF})\left(\frac{1}{4096}\right)$

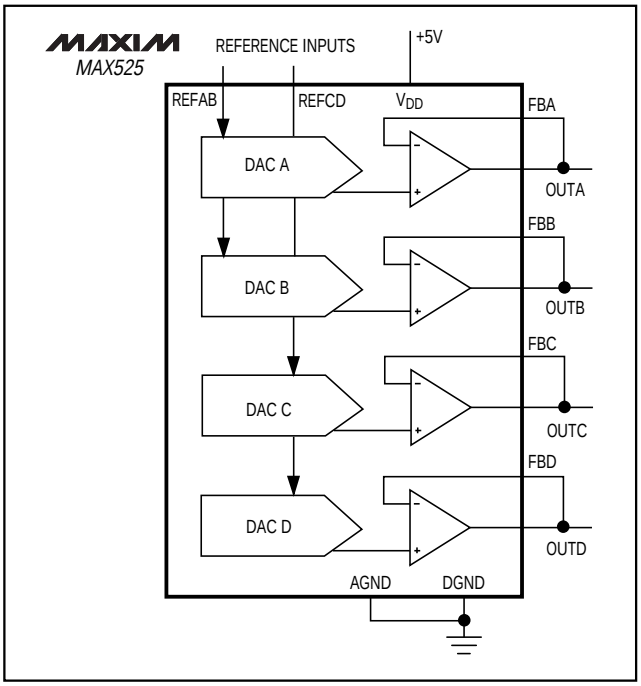


Figure 9. Unipolar Output Circuit

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

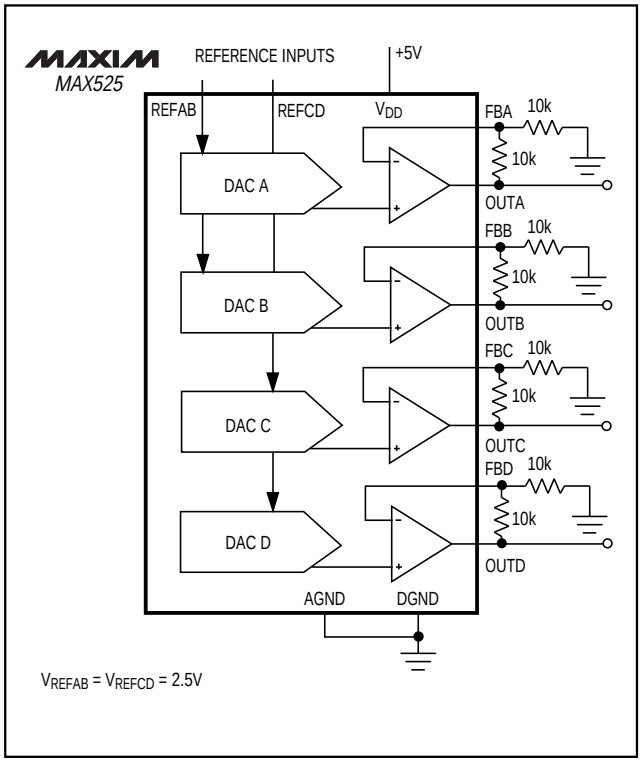


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX525 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX525's total harmonic distortion plus noise (THD + N) is typically less than -72dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

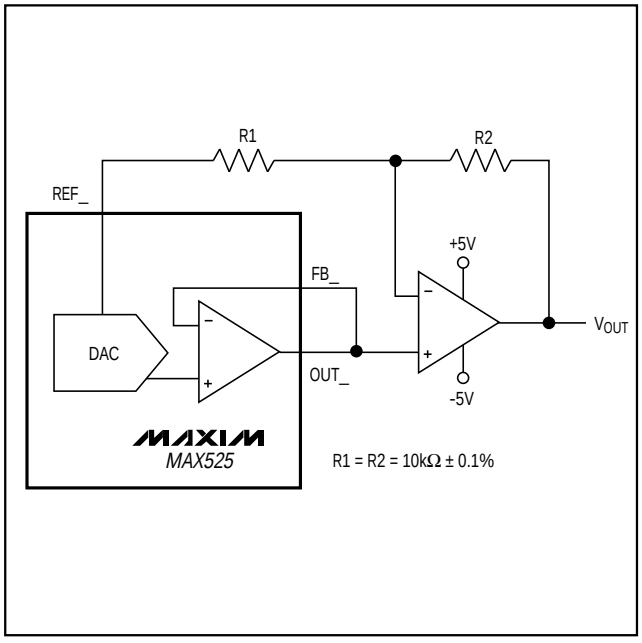


Figure 11. Bipolar Output Circuit

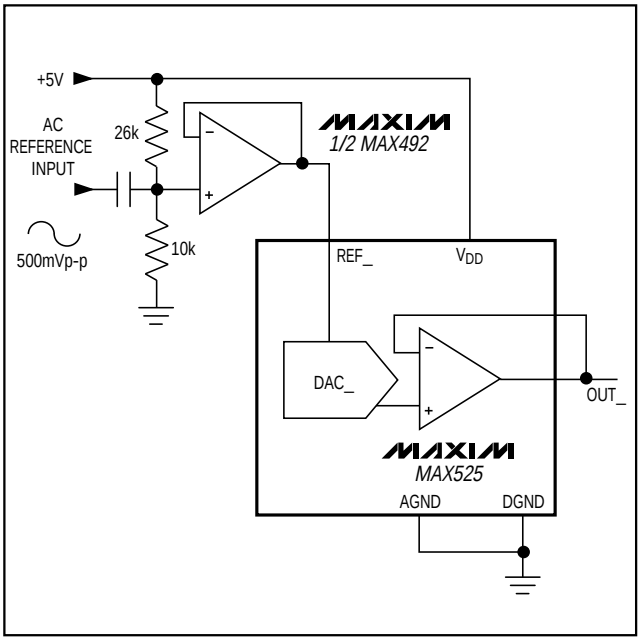


Figure 12. AC Reference Input Circuit

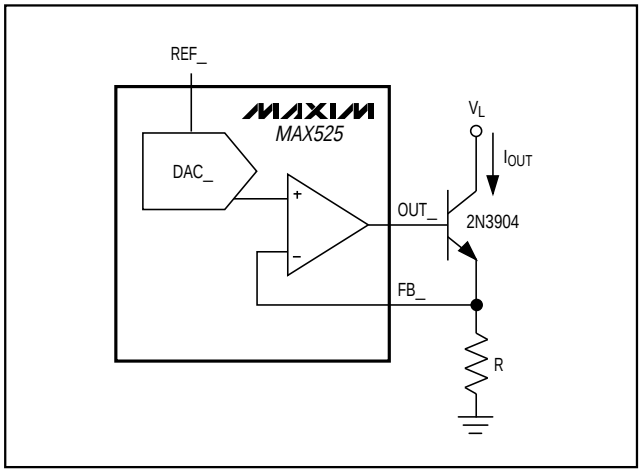


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

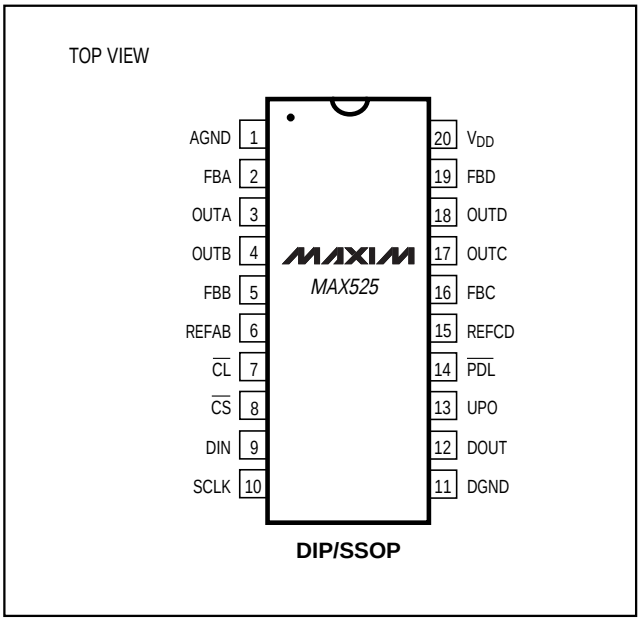
For rated MAX525 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Ordering Information (continued)

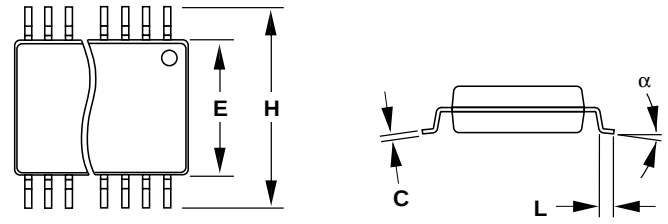
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX525BC/D	0°C to +70°C	Dice*	±1
MAX525AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX525BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX525AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX525BEAP	-40°C to +85°C	20 SSOP	±1
MAX525AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX525BMJP	-55°C to +125°C	20 CERDIP**	±1

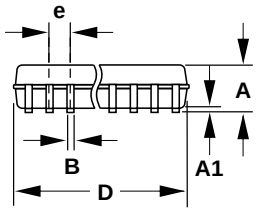
** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 4337

Package Information





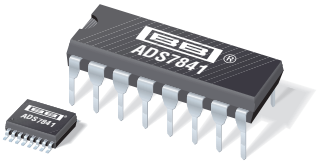
SSOP SHRINK SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

ADS7841



SBOS084A – NOVEMBER 2000

12-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- ±1 LSB MAX INL AND DNL
- GUARANTEED NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- DIP-16 OR SSOP-16 PACKAGE
- ALTERNATE SOURCE FOR MAX1247

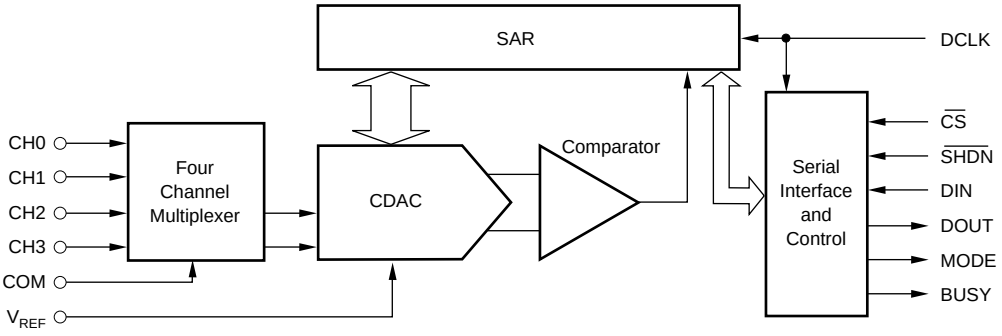
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS7841 is a 4-channel, 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 bits or 12 bits. Typical power dissipation is 2mW at a 200kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 100mV and V_{CC}, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode which reduces power dissipation to under 15µW. The ADS7841 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a DIP-16 or a SSOP-16 package and is guaranteed over the –40°C to +85°C temperature range.



SPECIFICATION: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+1.25	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–80	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	79		76	81		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		120			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	3.0		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900			*	µA
	f_{SAMPLE} = 12.5kHz		300			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				4.5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

SPECIFICATION: +2.7V

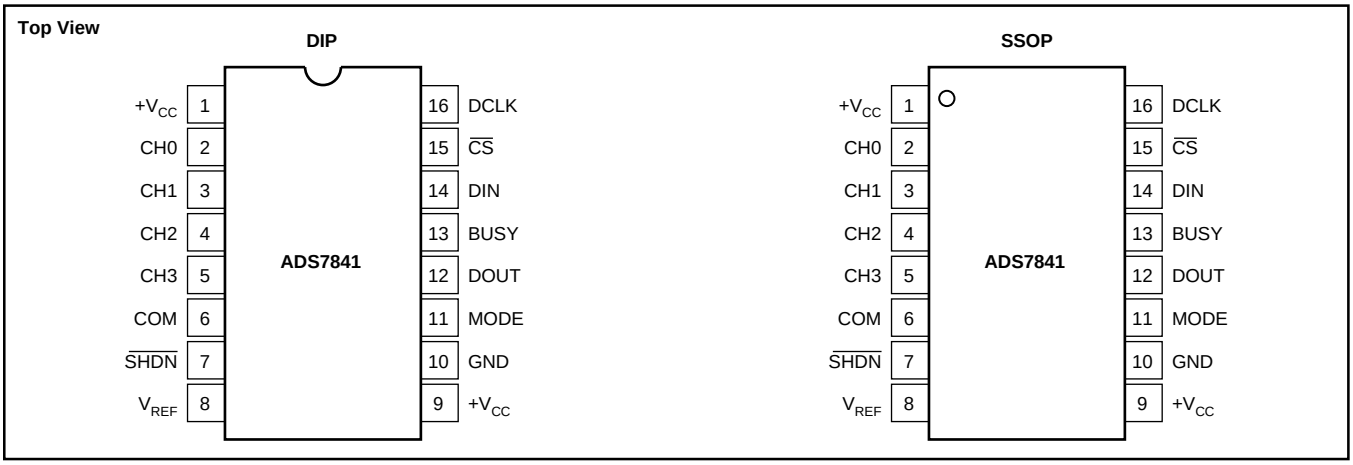
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 10kHz		–77	–72		–79	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 2.5Vp-p at 10kHz	72	78		76	80		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_{CC}$	Power Supply, 2.7V to 5V.
2	CH0	Analog Input Channel 0.
3	CH1	Analog Input Channel 1.
4	CH2	Analog Input Channel 2.
5	CH3	Analog Input Channel 3.
6	COM	Ground Reference for Analog Inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point.
7	$\overline{SHDN}$	Shutdown. When LOW, the device enters a very low power shutdown mode.
8	V_{REF}	Voltage Reference Input
9	$+V_{CC}$	Power Supply, 2.7V to 5V.
10	GND	Ground
11	MODE	Conversion Mode. When LOW, the device always performs a 12-bit conversion. When HIGH, the resolution is set by the MODE bit in the CONTROL byte.
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

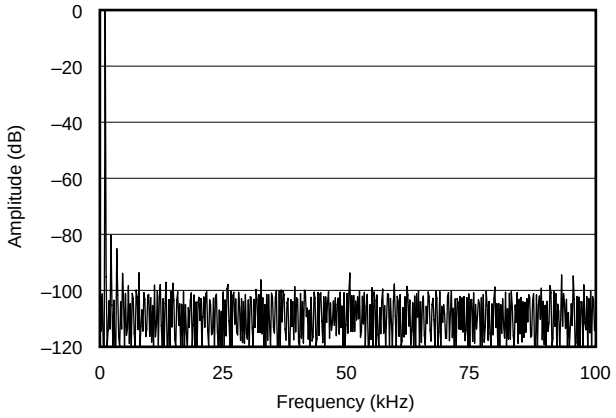
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS7841E	±2	±4	–40°C to +85°C	16-Lead SSOP	322	ADS7841E	Rails
"	"	"	"	"	"	ADS7841E/2K5	Tape and Reel
ADS7841P	±2	"	–40°C to +85°C	16-Pin PDIP	180	ADS7841P	Rails
ADS7841EB	±1	±3	–40°C to +85°C	16-Lead SSOP	322	ADS7841EB	Rails
"	"	"	"	"	"	ADS7841EB/2K5	Tape and Reel
ADS7841PB	±1	"	–40°C to +85°C	16-Pin PDIP	180	ADS7841PB	Rails

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7841E/2K5" will get a single 2500-piece Tape and Reel.

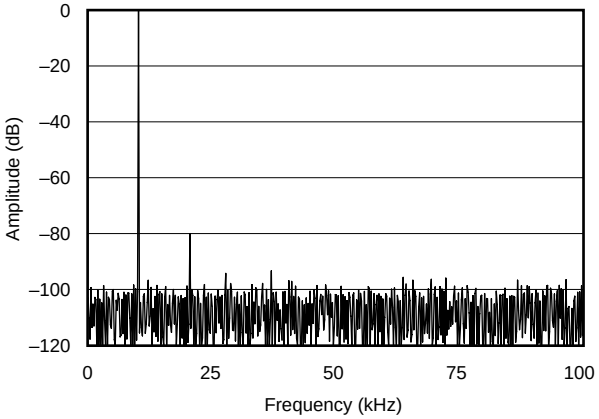
TYPICAL PERFORMANCE CURVES:+5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

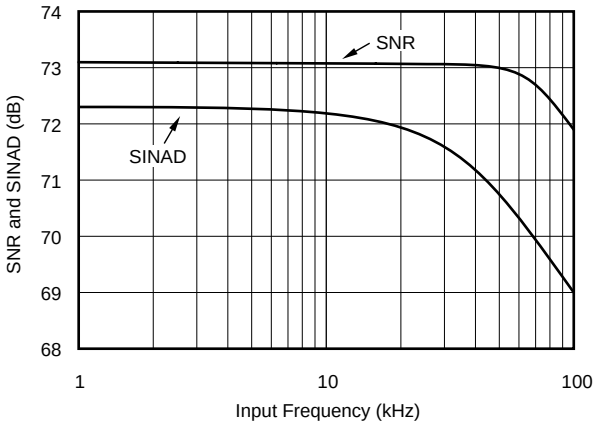
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



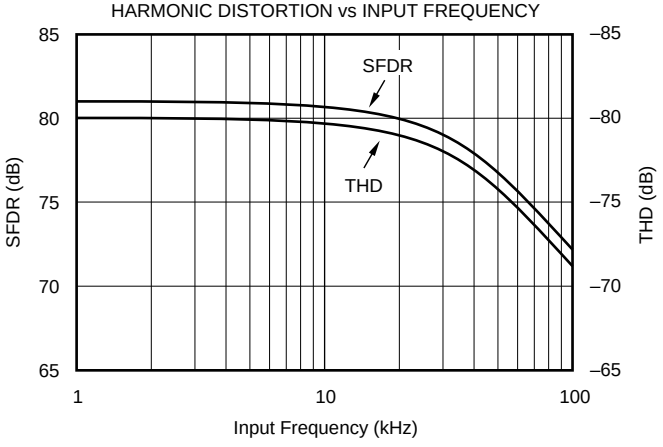
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



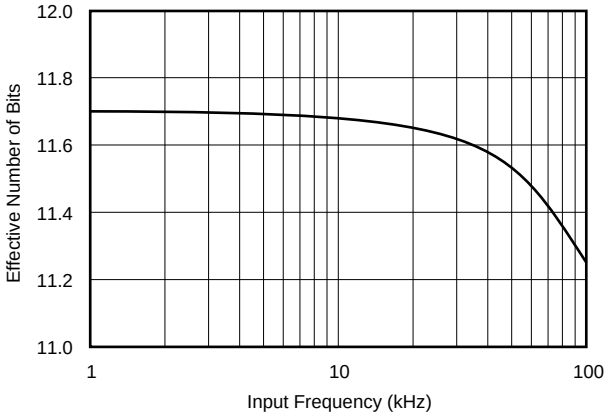
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



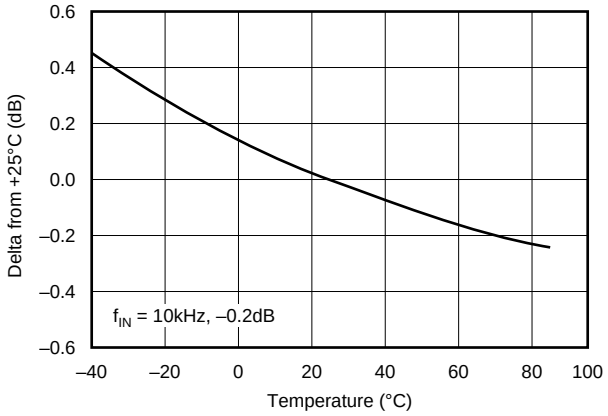
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



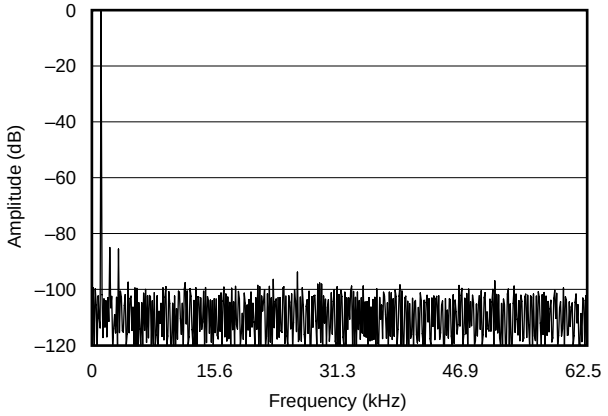
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



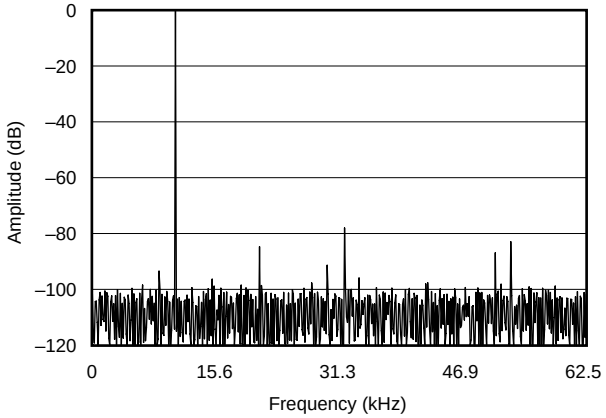
TYPICAL PERFORMANCE CURVES:+2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

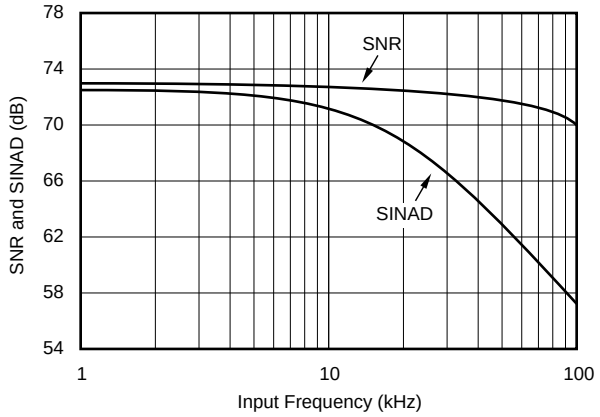
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



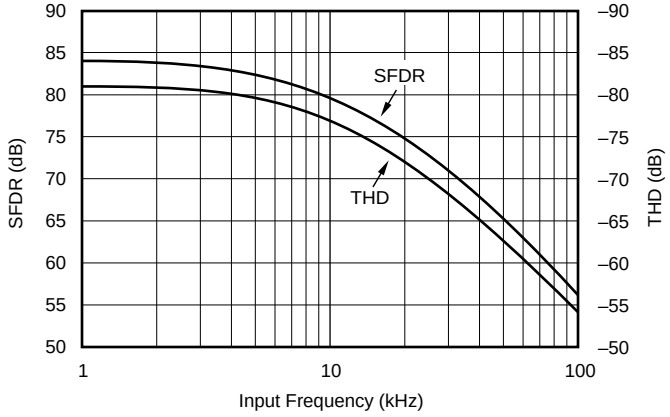
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



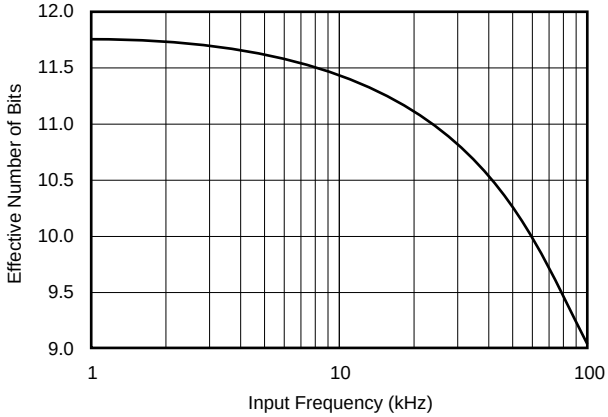
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



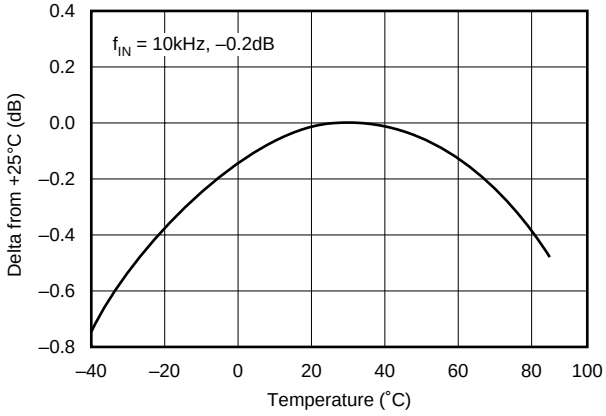
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



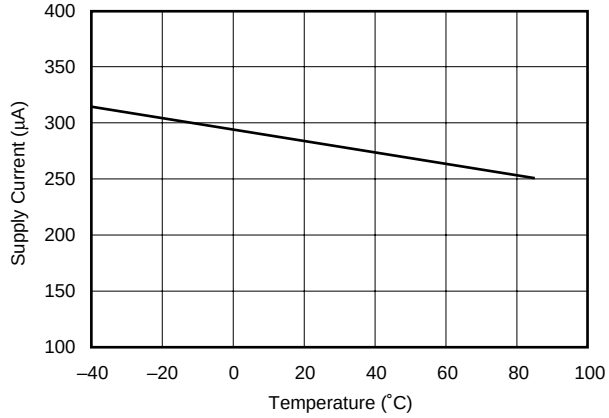
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



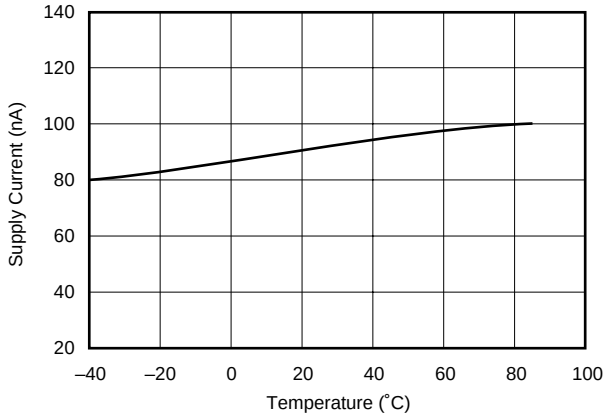
TYPICAL PERFORMANCE CURVES:+2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

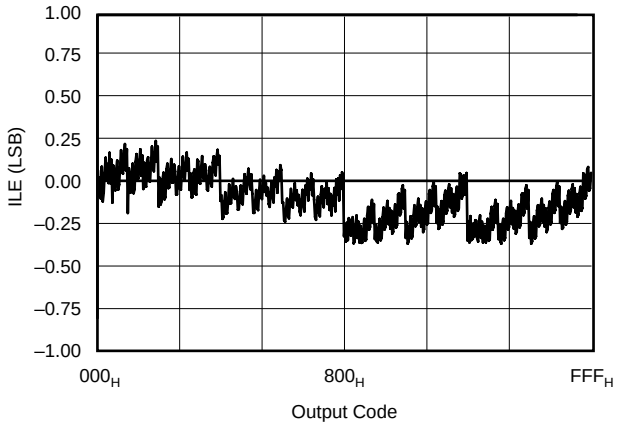
SUPPLY CURRENT vs TEMPERATURE



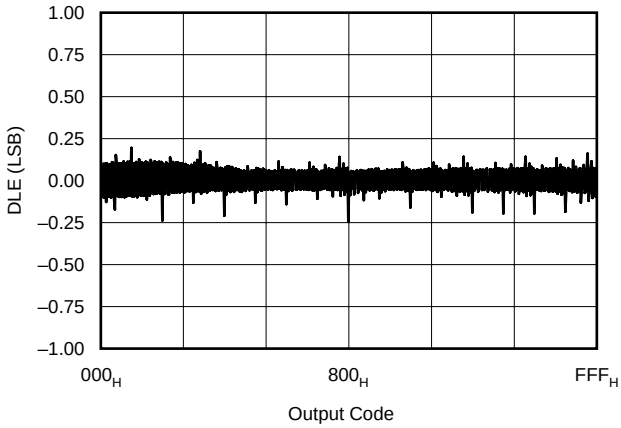
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



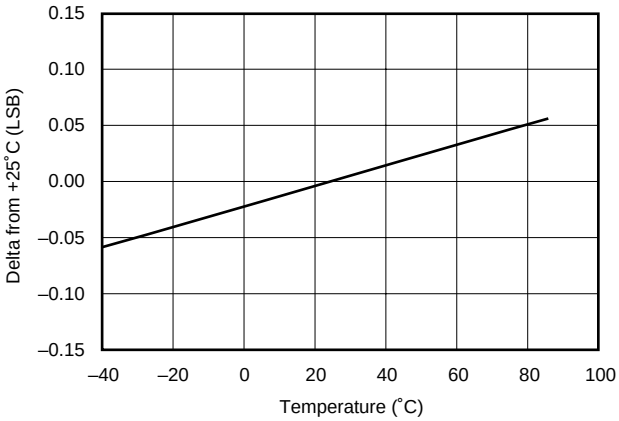
INTEGRAL LINEARITY ERROR vs CODE



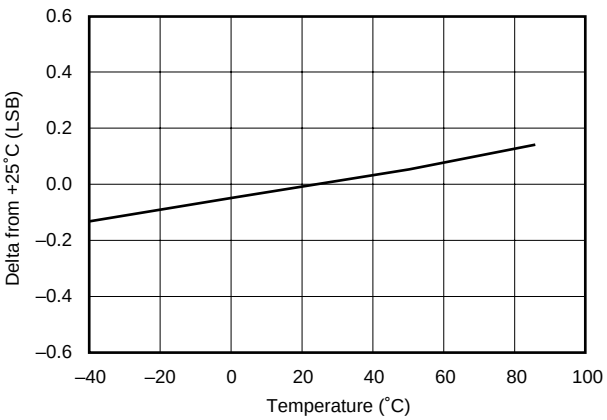
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



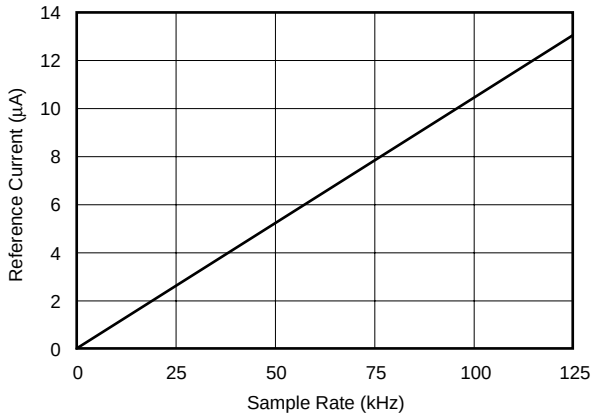
CHANGE IN OFFSET vs TEMPERATURE



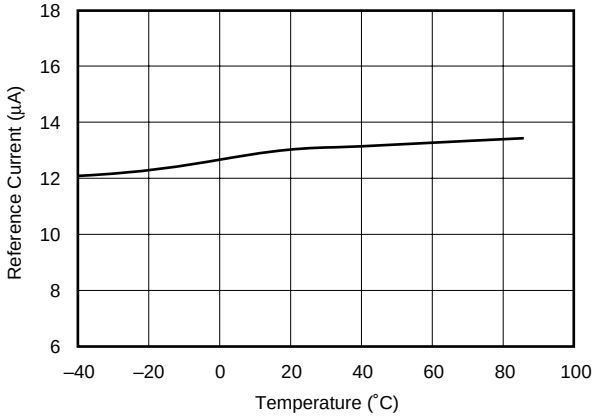
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

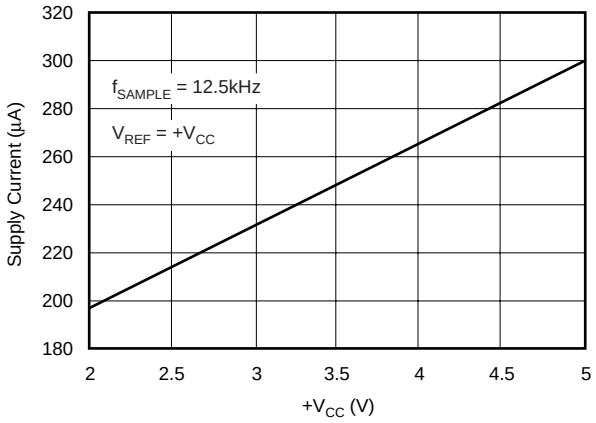
REFERENCE CURRENT vs SAMPLE RATE



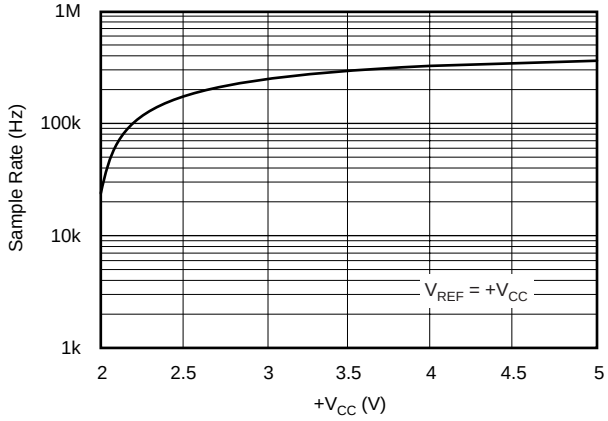
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7841 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

The analog input to the converter is differential and is provided via a four-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using two of the four input channels (CH0 - CH3). The particular configuration is selectable via the digital interface.

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/$\overline{\text{DIF}}$ control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2V and 1.25V, allowing the input to reject small signals which are common to both the +IN and –IN input. The +IN input has a range of –0.2V to $+V_{CC}$ + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				–IN
1	0	1		+IN			–IN
0	1	0			+IN		–IN
1	1	0				+IN	–IN

TABLE I. Single-Ended Channel Selection (SGL/$\overline{\text{DIF}}$ HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	–IN			
1	0	1	–IN	+IN			
0	1	0			+IN	–IN	
1	1	0			–IN	+IN	

TABLE II. Differential Channel Control (SGL/$\overline{\text{DIF}}$ LOW).

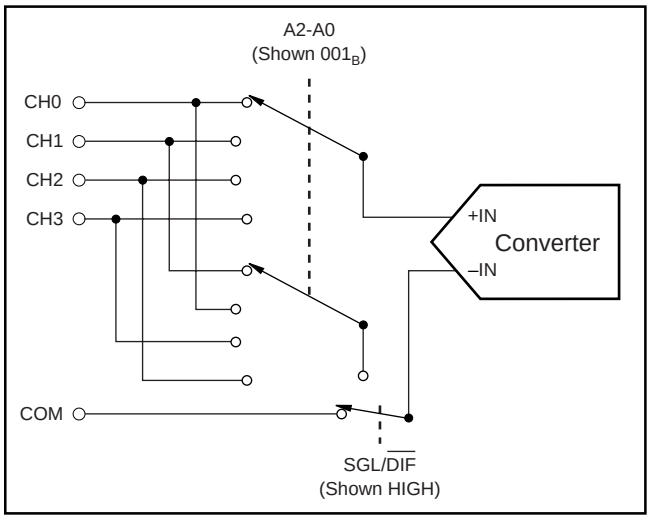


FIGURE 2. Simplified Diagram of the Analog Input.

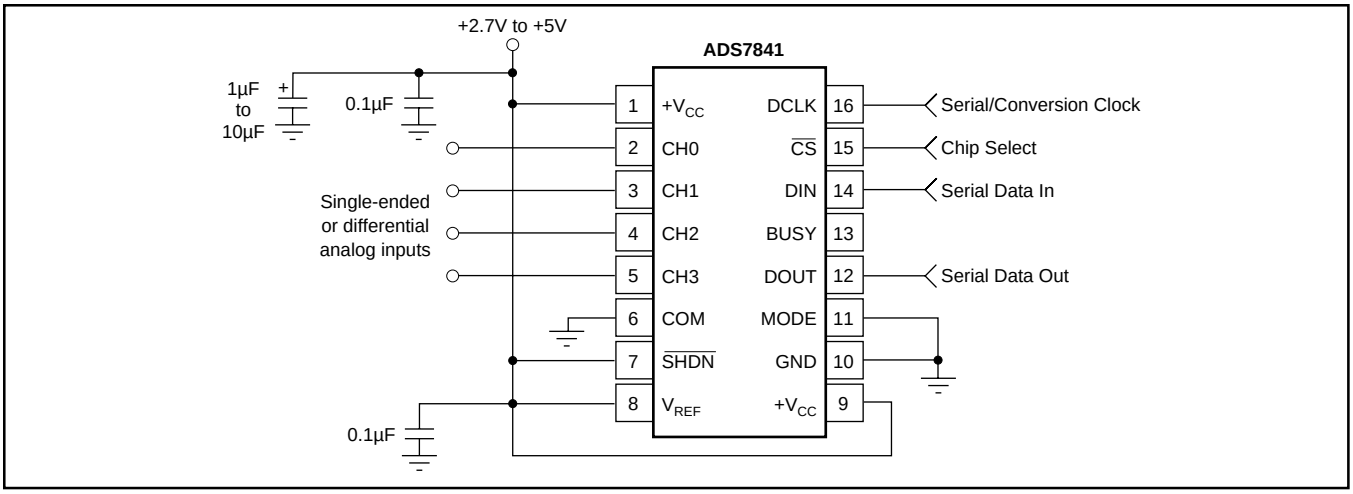


FIGURE 1. Basic Operation of the ADS7841.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7841 will operate with a reference in the range of 100mV to $+V_{CC}$. Keep in mind that the analog input is the difference between the +IN input and the –IN input as shown in Figure 2. For example, in the single-ended mode, a 1.25V reference, and with the COM pin grounded, the selected input channel (CH0 - CH3) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5V reference, then it will typically be 10 LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7841. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of $+V_{CC}$). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample/hold goes into the hold mode. The next twelve clock cycles accomplish the actual analog-to-digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

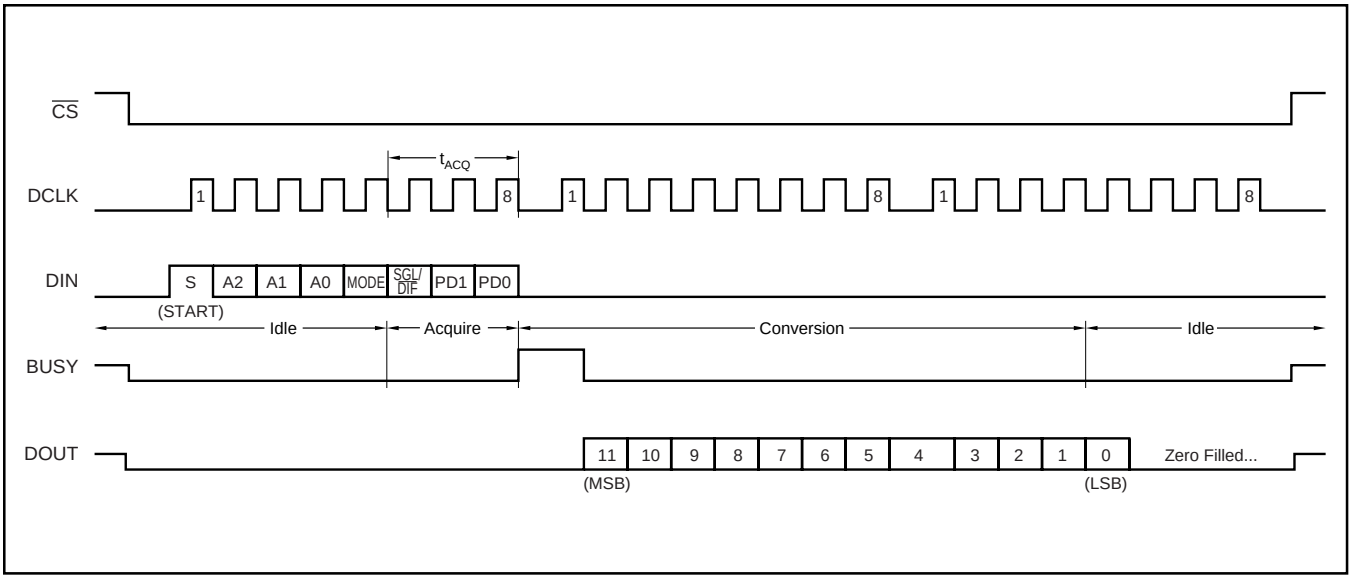


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7841 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input as detailed in Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. If the MODE pin is HIGH, this bit controls the number of bits for the next conversion: 12-bits (LOW) or 8-bits (HIGH). If the MODE pin is LOW, this bit has no function and the conversion is always 12 bits.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input as detailed in Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is LOW, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is HIGH, then the MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SGL/$\overline{\text{DIF}}$ bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

16-Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample/hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.

PD1	PD0	Description
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved for future use.
1	0	Reserved for future use.
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

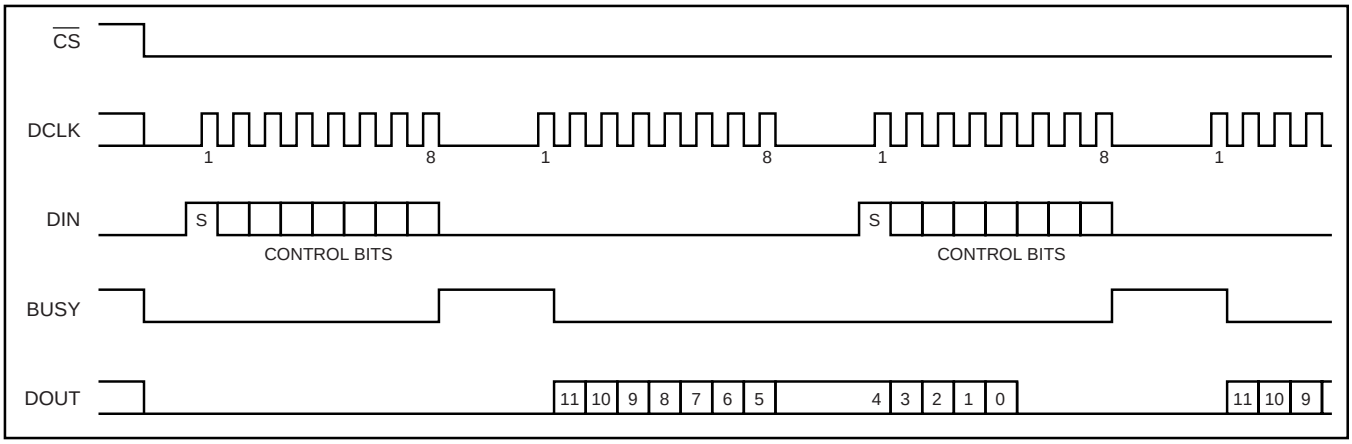


FIGURE 4. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

Digital Timing

Figure 5 and Tables VI and VII provide detailed timing for the digital interface of the ADS7841.

15-Clocks per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	900			ns
t_{DS}	DIN Valid Prior to DCLK Rising	50			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

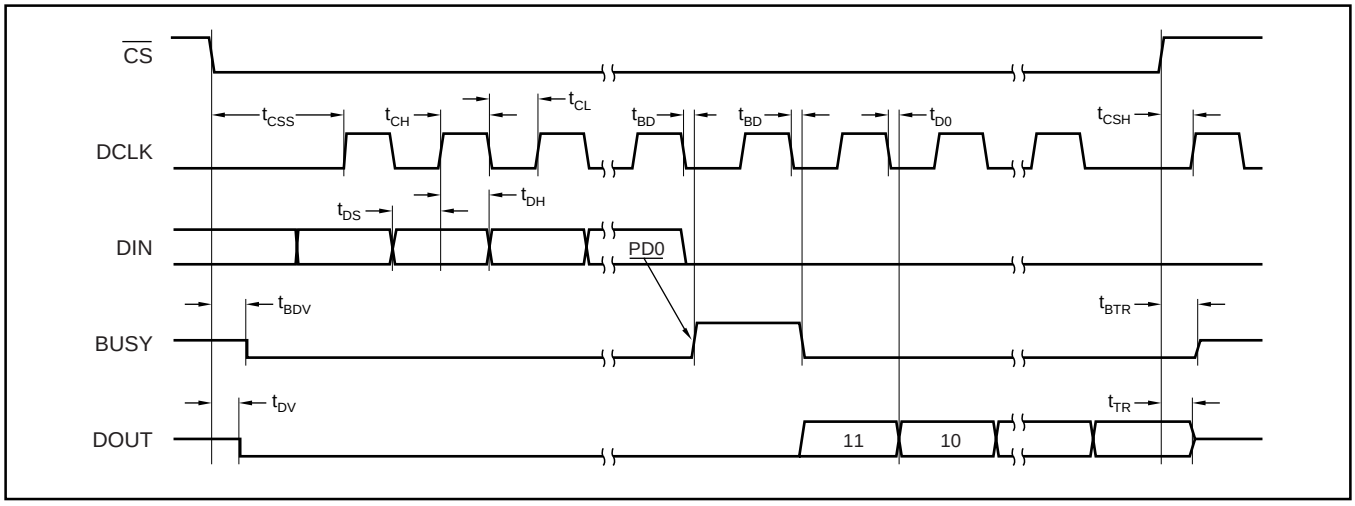


FIGURE 5. Detailed Timing Diagram.

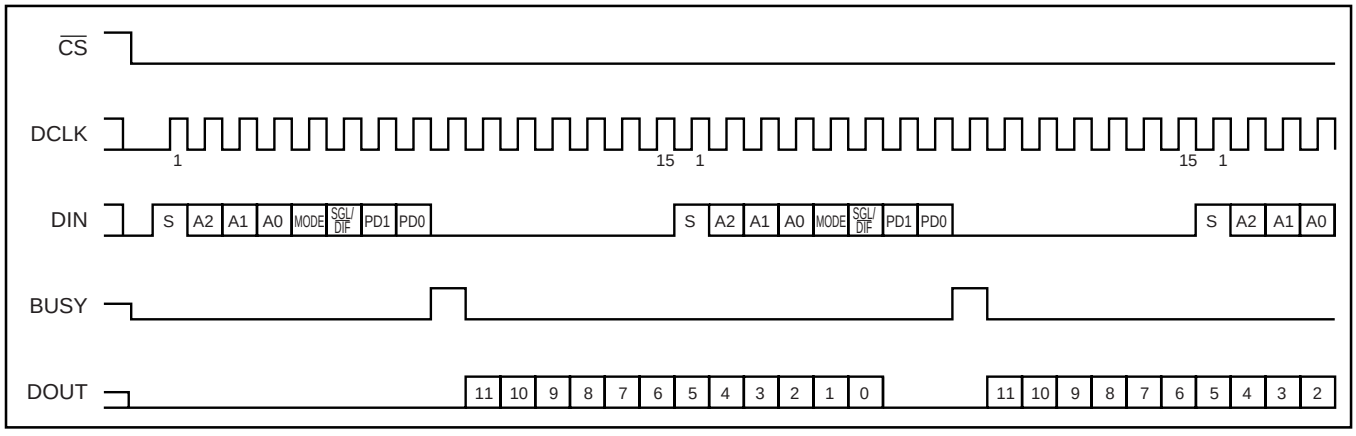


FIGURE 6. Maximum Conversion Rate, 15-Clocks per Conversion.

Data Format

The ADS7841 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

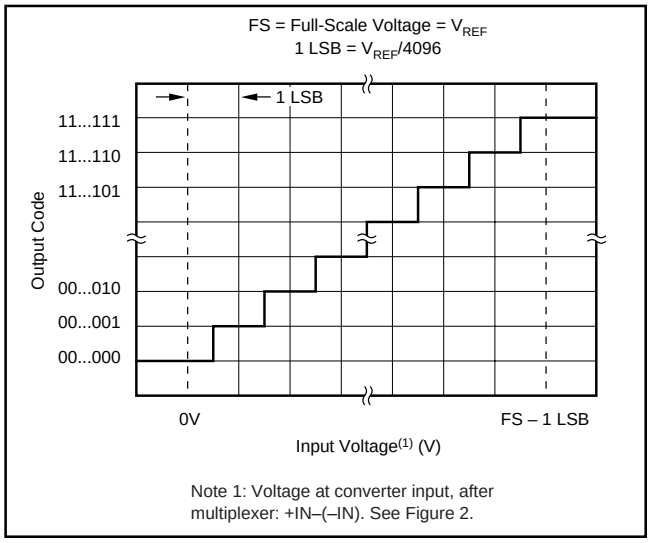


FIGURE 7. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The ADS7841 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide a 12-bit transfer or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7841 is not as critical, settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

POWER DISSIPATION

There are three power modes for the ADS7841: full power (PD1 - PD0 = 11B), auto power-down (PD1 - PD0 = 00B), and shutdown ($\overline{SHDN}$ LOW). The affects of these modes varies depending on how the ADS7841 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown ($\overline{SHDN}$ LOW) will not lower power dissipation.

When operating at full-speed and 16-clocks per conversion (as shown in Figure 4), the ADS7841 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and $\overline{CS}$ is LOW while the ADS7841 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ HIGH. The differences in supply current for these two cases are shown in Figure 9.

Operating the ADS7841 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. $\overline{SHDN}$ can be used to force an immediate power-down.

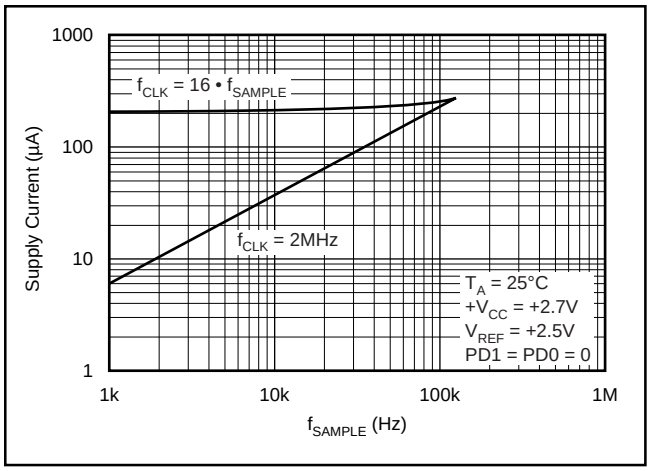


FIGURE 8. Supply Current vs Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

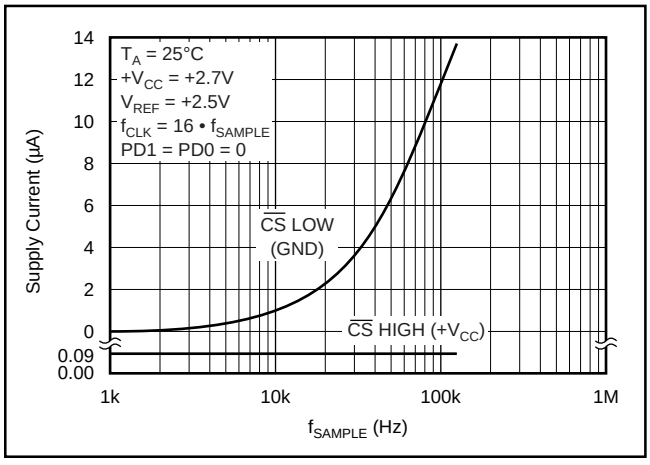


FIGURE 9. Supply Current vs State of $\overline{CS}$.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7841 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7841 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7841 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7841 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

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MAXIM

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.5µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E–MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications that are not ESD sensitive see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **ESD Protection: ±15kV—Human Body Model**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)**
- **Low Quiescent Current:**
  120µA (MAX483E/487E/488E/489E)
  230µA (MAX1487E)
  300µA (MAX481E/485E/490E/491E)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (Y, Z; A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487EC_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487EE_ A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 8		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 8				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487E/MAX1487E, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487E/MAX1487E		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487E/MAX1487E		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481E/MAX485E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483E/MAX487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	MAX483E		350	650	
				MAX487E		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V_{CC}				0.5	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model				±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	40	60	ns
	t_{PHL}			10	40	60	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	3	20	40	ns
			MAX490EC/E, MAX491EC/E	5	20	25	
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed			45	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed			45	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed			45	70	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed			45	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	20	60	200	ns
			MAX490EC/E, MAX491EC/E	20	60	150	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481E (Note 5)		50	200	600	ns

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 11 and 13, C_L = 100pF, S2 closed		45	100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 11 and 13, C_L = 100pF, S1 closed		45	100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 9 and 15, C_L = 15pF, S2 closed, A - B = 2V		225	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 9 and 15, C_L = 15pF, S1 closed, B - A = 2V		225	1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483E/MAX487E (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S1 closed			2500	ns

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.

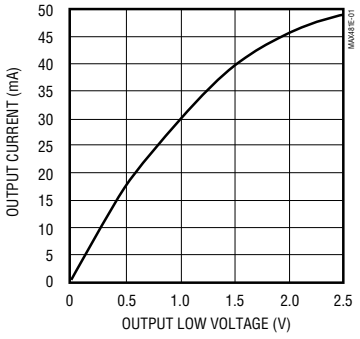
Note 4: Applies to peak current. See *Typical Operating Characteristics*.

Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

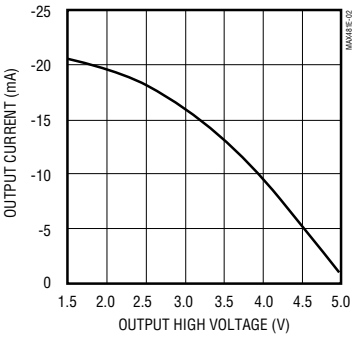
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

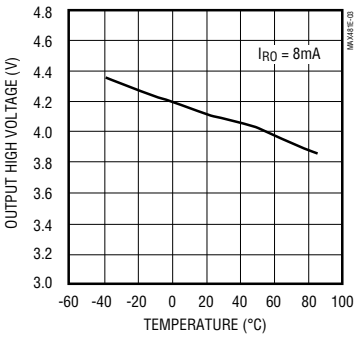
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



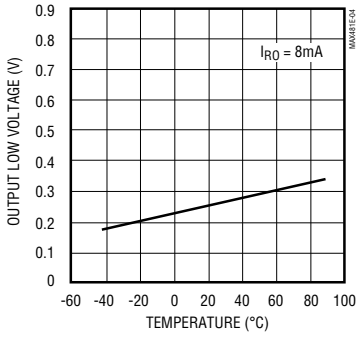
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



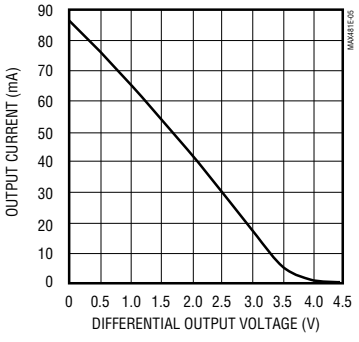
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE

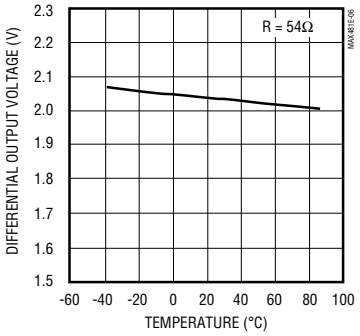


±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

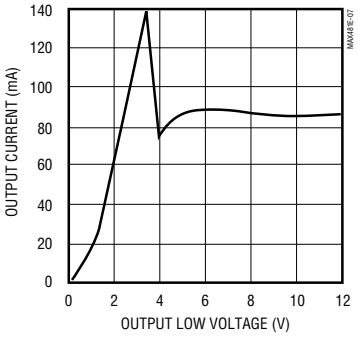
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

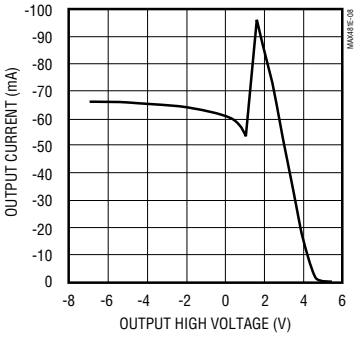
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



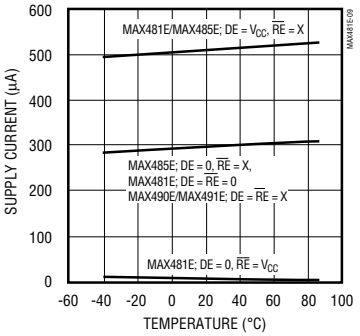
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



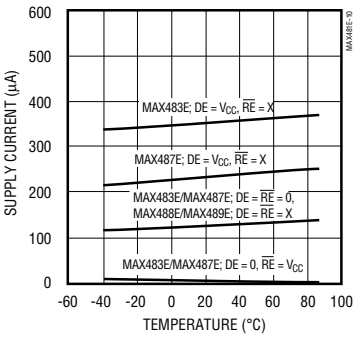
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



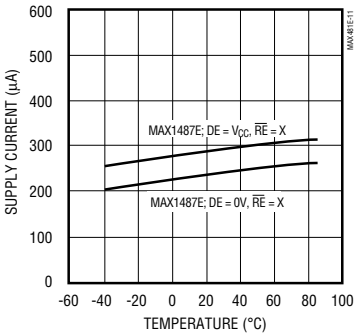
MAX481E/MAX485E/MAX490E/MAX491E SUPPLY CURRENT vs. TEMPERATURE



MAX483E/MAX487E–MAX489E SUPPLY CURRENT vs. TEMPERATURE



MAX1487E SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E	MAX488E MAX490E	MAX489E MAX491E		
1	2	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	4	6, 7	GND	Ground
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	14	V_{CC}	Positive Supply: 4.75V ≤ V_{CC} ≤ 5.25V
—	—	1, 8, 13	N.C.	No Connect—not internally connected

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

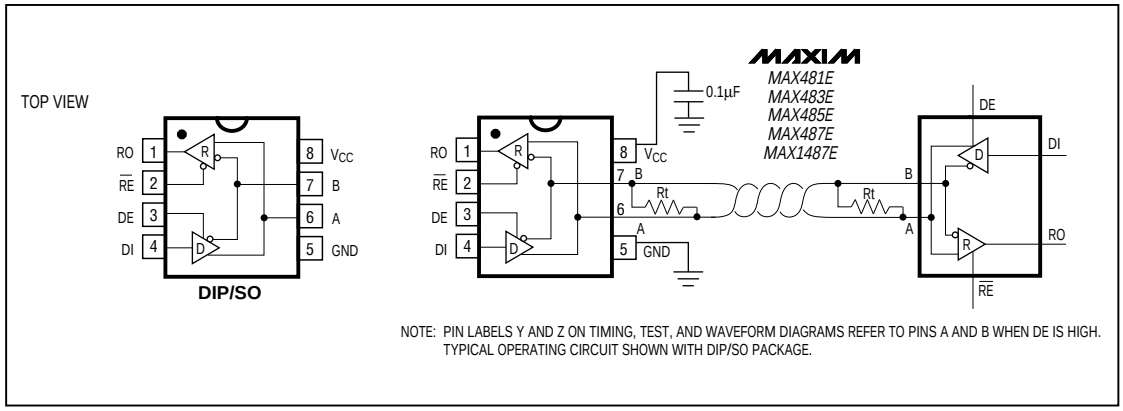


Figure 1. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Pin Configuration and Typical Operating Circuit

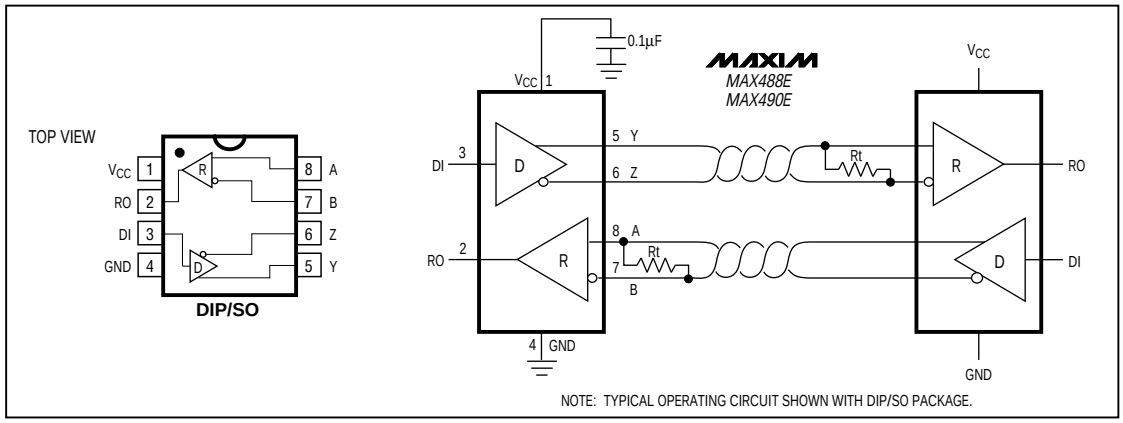


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

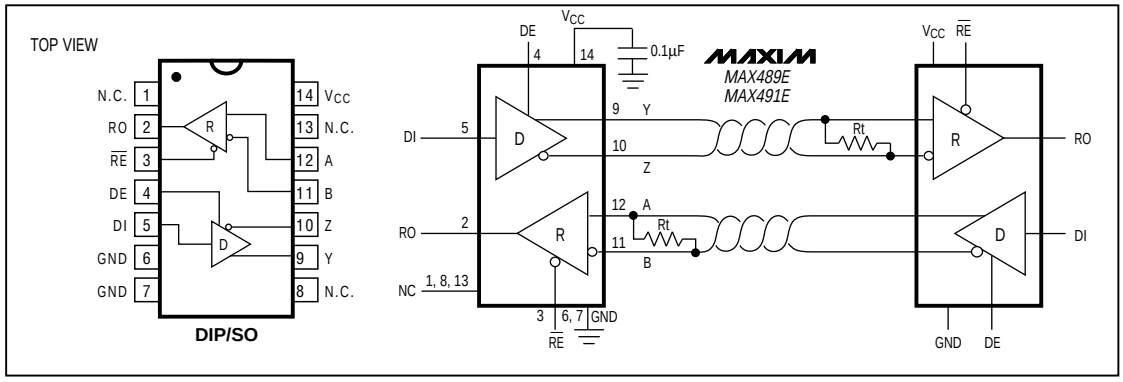


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E–MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX497E–MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E–MAX491E are full-duplex transceivers, while the MAX481E, MAX483E, MAX487E, and MAX1487E are half-duplex. In addition, driver-enable (DE) and receiver-enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).

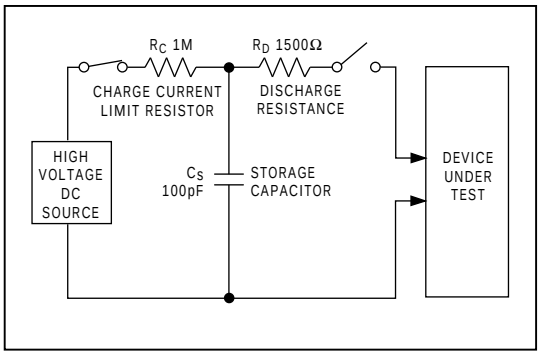


Figure 4. Human Body ESD Test Model

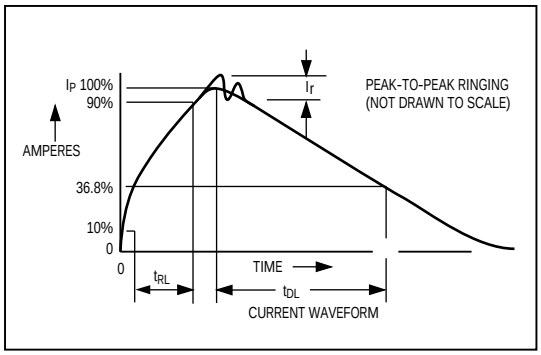


Figure 5. Human Body Model Current Waveform

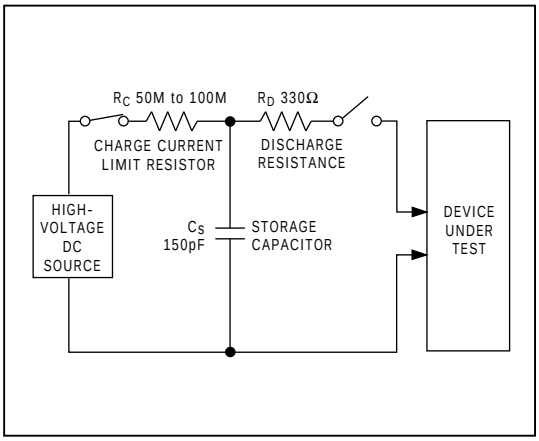


Figure 6. IEC1000-4-2 ESD Test Model

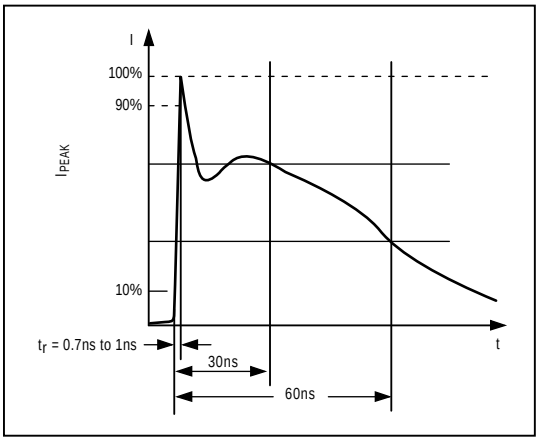


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

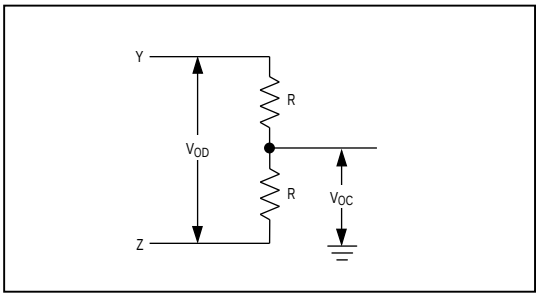


Figure 8. Driver DC Test Load

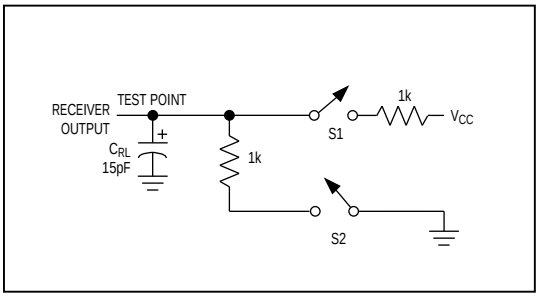


Figure 9. Receiver Timing Test Load

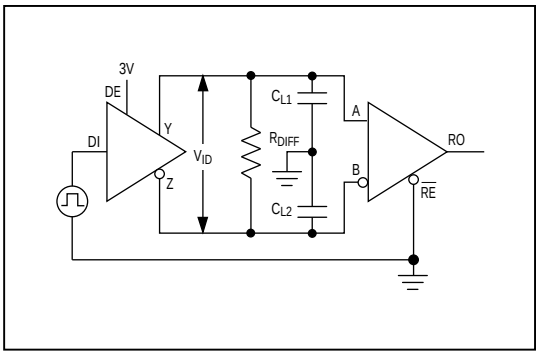


Figure 10. Driver/Receiver Timing Test Circuit

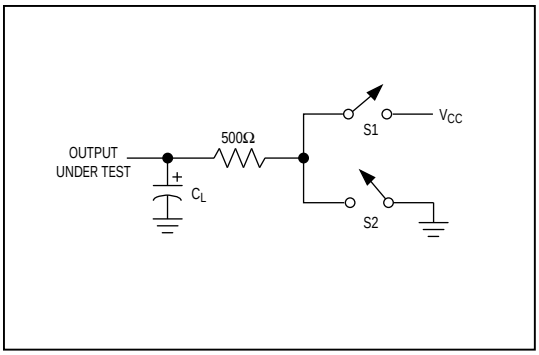


Figure 11. Driver Timing Test Load

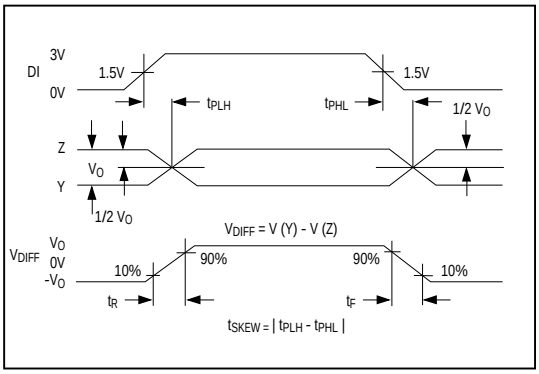


Figure 12. Driver Propagation Delays

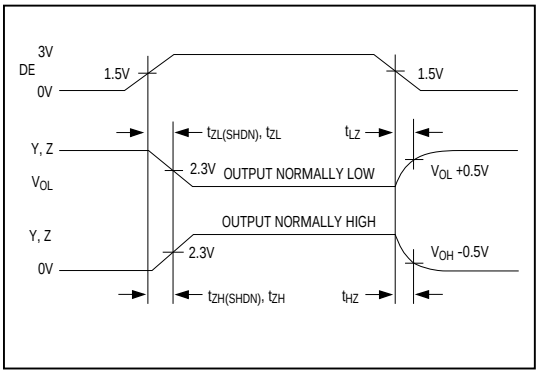


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

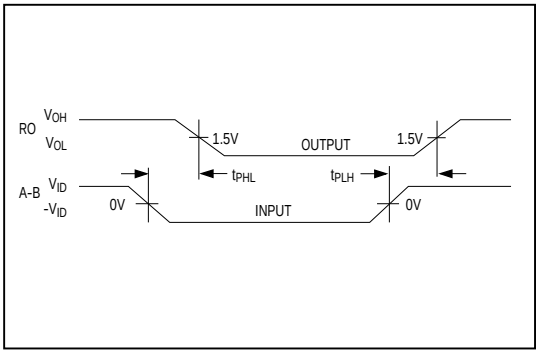


Figure 14. Receiver Propagation Delays

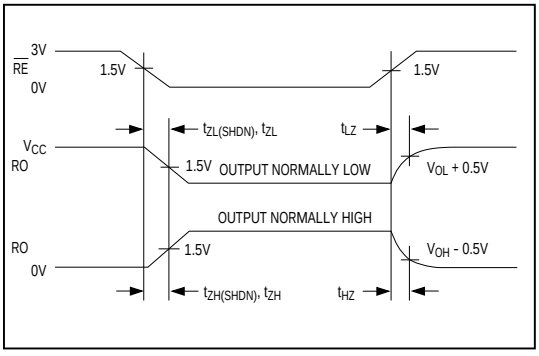


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

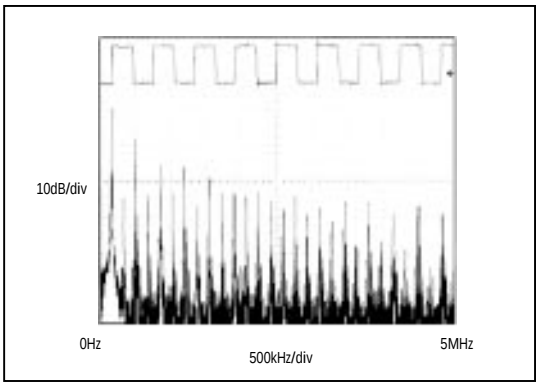


Figure 16. Driver Output Waveform and FFT Plot of MAX485E/MAX490E/MAX491E/MAX1487E Transmitting a 150kHz Signal

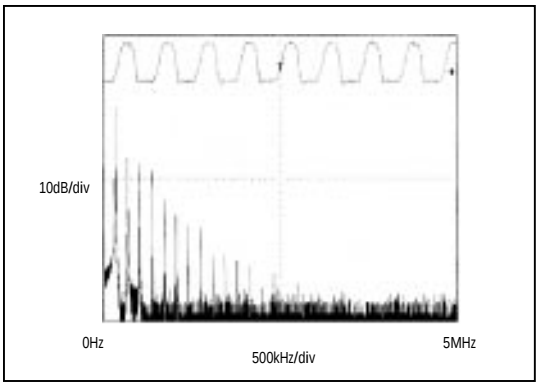


Figure 17. Driver Output Waveform and FFT Plot of MAX483E/MAX487E–MAX489E Transmitting a 150kHz Signal

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E–MAX491E have standard 12kΩ receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E–MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 16 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481E, MAX485E, MAX490E, MAX491E, or MAX1487E. High-frequency harmonics with large amplitudes are evident. Figure 17 shows the same information displayed for a MAX483E, MAX487E, MAX488E, or MAX489E transmitting under the same conditions. Figure 17's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.5µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485E, MAX488E–MAX491E, and MAX1487E can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

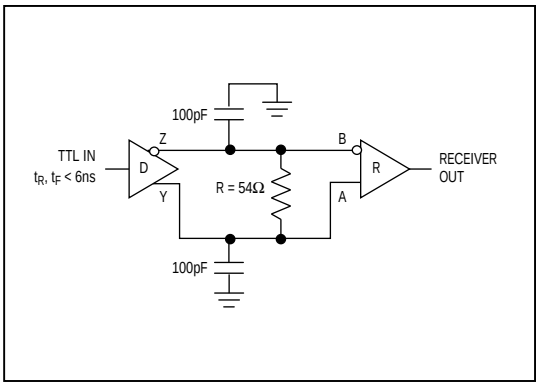


Figure 18. Receiver Propagation Delay Test Circuit

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 19–22 using Figure 18's test circuit.

The difference in receiver delay times, t_{PLH} - t_{PHL}, is typically under 13ns for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and is typically less than 100ns for the MAX483E and MAX487E–MAX489E.

The driver skew times are typically 5ns (10ns max) for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and are typically 100ns (800ns max) for the MAX483E and MAX487E–MAX489E.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 25 and 26 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E–MAX489E are more tolerant of imperfect termination. Bypass the V_{CC} pin with 0.1µF.

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. Figures 23 and 24 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 100Ω loads.

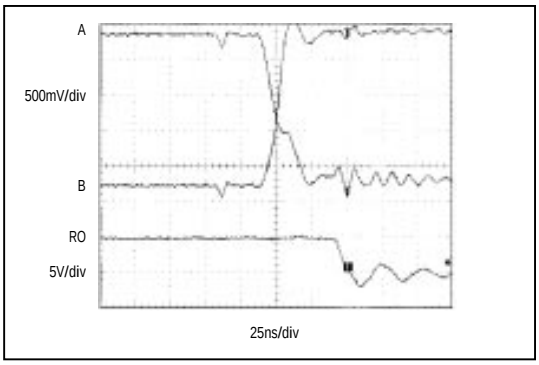


Figure 19. MAX481E/MAX485E/MAX490E/MAX1487E Receiver t_{PHL}

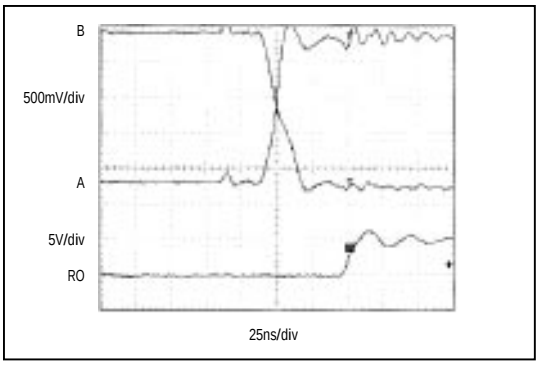


Figure 20. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E Receiver t_{PLH}

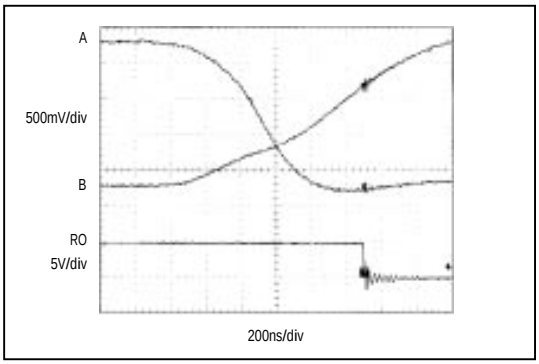


Figure 21. MAX483E/MAX487E–MAX489E Receiver t_{PHL}

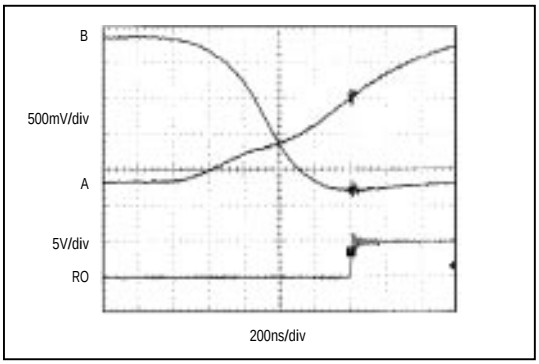


Figure 22. MAX483E/MAX487E–MAX489E Receiver t_{PLH}

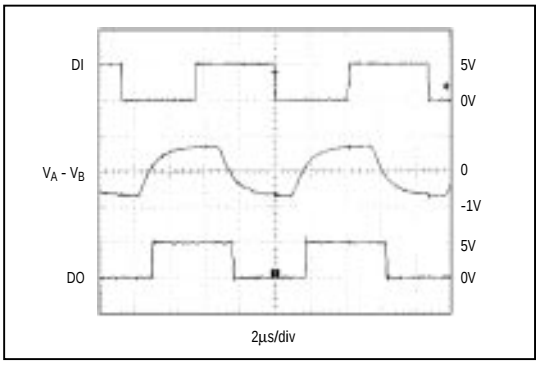


Figure 23. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E System Differential Voltage at 110kHz Driving 4000ft of Cable

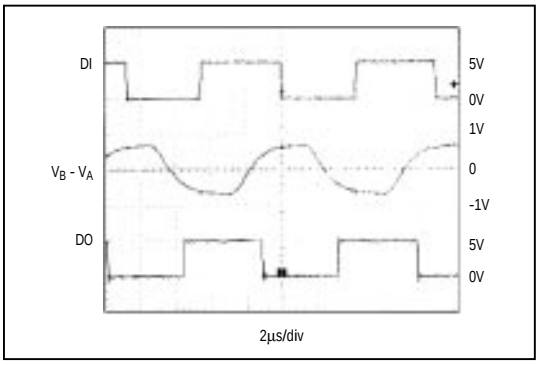


Figure 24. MAX483E/MAX1487E–MAX489E System Differential Voltage at 110kHz Driving 4000ft of Cable

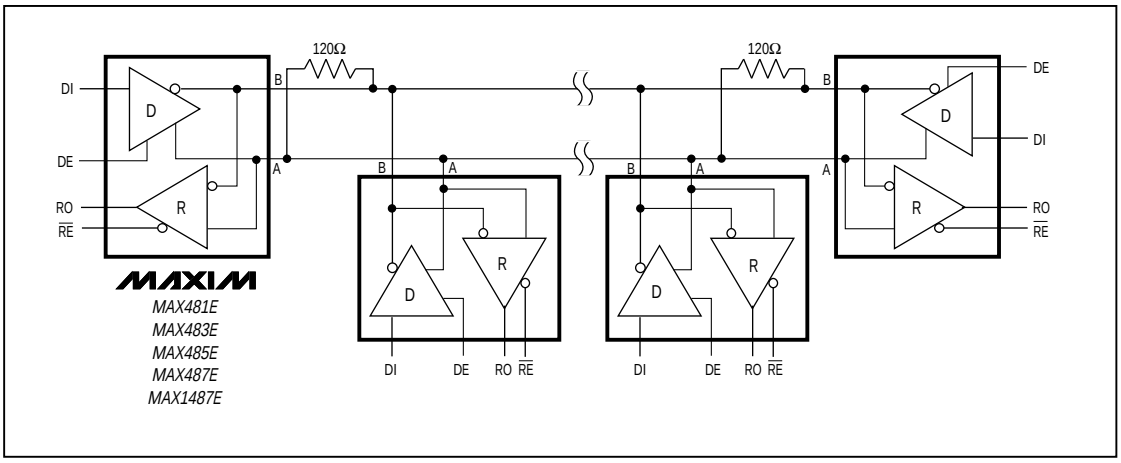


Figure 25. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

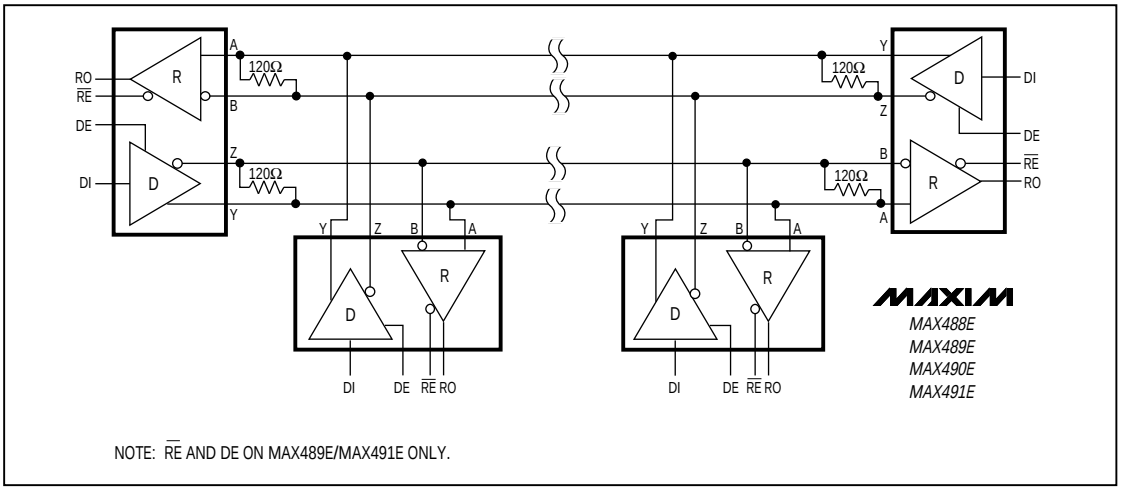


Figure 26. MAX488E–MAX491E Full-Duplex RS-485 Network

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSD	0°C to +70°C	14 SO
MAX489EEPD	-40°C to +85°C	14 Plastic DIP
MAX489EESD	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSD	0°C to +70°C	14 SO
MAX491EEPD	-40°C to +85°C	14 Plastic DIP
MAX491EESD	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 295