Appendix D - Data Sheets Of Key Components

- MTRX192L Optical receiver Module Multiplex Inc

  Application Note on feedback loop
- PT422x DC-DC Converter Power Trends (TI)

  Application Note on remote control and voltage adjustment
- MC78L08 Linear 8volt regulator ON semiconductor
- MAX525 Digital to Analog Converter Maxim
- ADS7841 Analog to Digital Converter Burr Brown Products (TI)
- LM4051 Voltage reference diode National Semiconductor
- LM61 Temperature sensor National Semiconductor
- MAX 487 RS422 Transceiver Maxim
- OPA241 Operational Amplifier Burr Brown (TI)
- MAX407 Operational Amplifier Maxim

MTRX192L

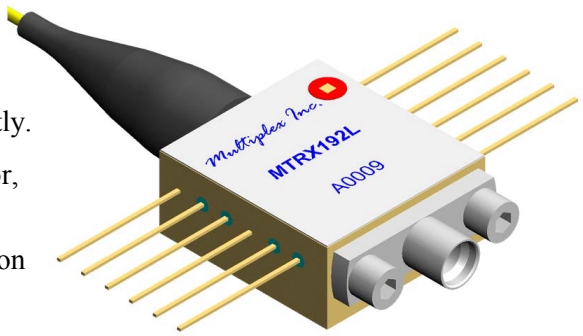
Multiplex, Inc.
Photonics for Communications

High performance optical receiver module including an output limiting amplifier for 10Gb/s system applications. Applicable to 12.5Gb/s.

Preliminary Datasheet

Features:

- MTRX192L: Optical receiver module including PIN diode, low noise TIA and limiting amplifier.
- Low power consumption.
- Data output interface either with coaxial connector or by soldering the RF feed through pin to the circuit board directly.
- Choice of output coaxial connector among: GPO© connector, K©-connector, or SMA connector.
- Non-inverted, single-end AC-couple output. (Package version with differential outputs available.)
- Choice of input optical connector of such as ST, FC-PC, etc.
- Operational Temperature: -20°C to + 80°C.



Note: GPO is the trademark of Gilbert Engineer Co., Inc. K-connector is the trademark of Anritsu/Wiltron.

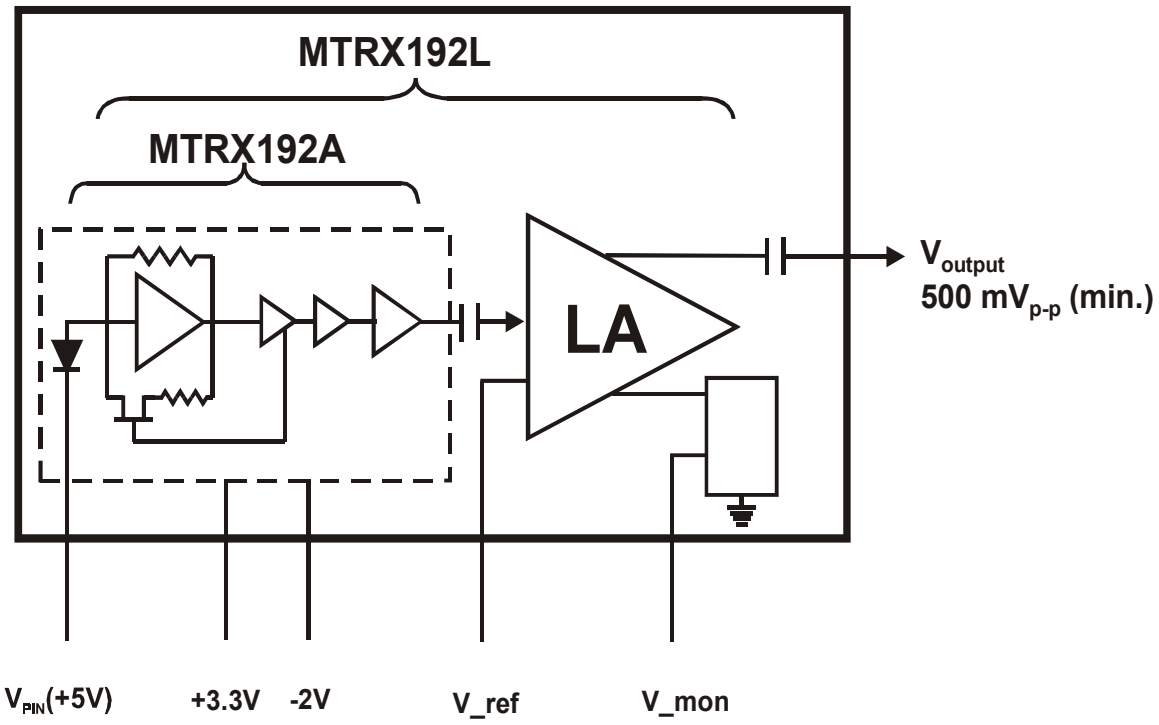
Performance Specifications:

Parameters	Unit	Min	Typ	Max	Comments/Test Conditions
Receiver sensitivity	dBm	-	-20	-19	10Gb/s. BER at $1x10^{-10}$. λ = 1.5mm
Maximum operational optical input power	dBm	0	-	-	λ=1.5μm; error free operation
PIN responsivity	A/W	0.75	> 0.8	-	λ=1.5μm
TIA transimpedance gain	Ω	1K	1.2K	-	Small signal gain
TIA 3dB Bandwidth	GHz	8	9	-	Small signal frequency response
Receiver low frequency cutoff (3dB)	kHz	-	< 50	100	-20°C to +85°C
TIA transfer function phase linearity deviation	degree	-	< 10	20	(100 kHz to 8 GHz)
TIA transfer function amplitude peaking	dB	-	< 1	1.5	(100 kHz to 9GHz)
Input optical reflectance	dB	-	<- 40	-30	For λ=1.3μm and 1.5μm; excluding reflection from optical connector.
Output Rise and Fall Time	ps	-	< 40	-	10% - 90%
Total Power consumption	mW	-	-	750	

DC Characteristics (MTRX192L):

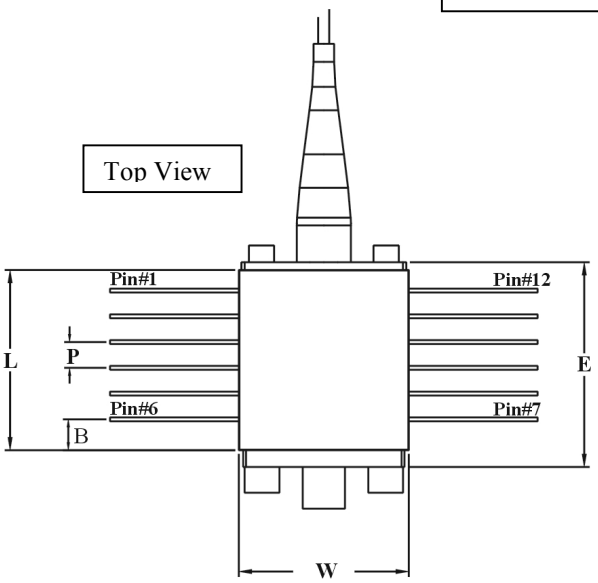
Parameters	Unit	Min	Typ	Max	Current (mA; Max)
PIN diode bias (Note-1)	V	+4.75	+5	+15	-
Positive receiver module bias	V	+3.0	+3.3	+3.6	110
Negative receiver module bias	V	-2.2	-2.0	-1.8	160

Note-1. All tests were performed with 5V reverse bias for the PIN photo diode. Increasing the PIN reverse bias to 10V will, in general, enhance the receiver sensitivity slightly.

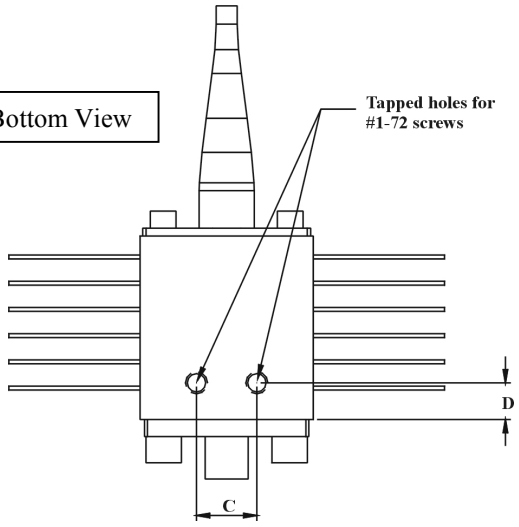


MTRX192L Physical dimensions

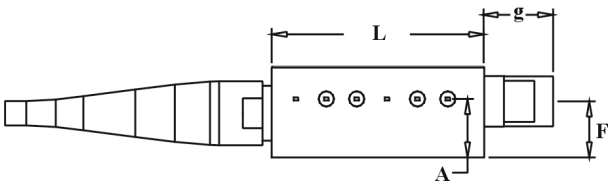
Top View

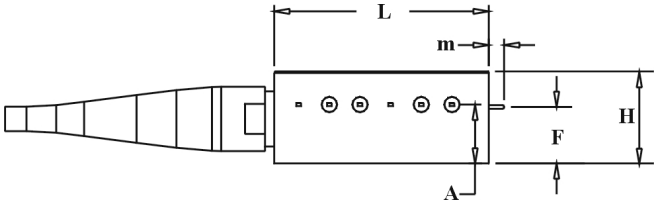


Bottom View



Side View with or without GPO connector





Pin Descriptions

Pin Number	MTRX192L
1	GND
2	V_PIN
3	-2.2V
4	GND
5	-2.2V
6	NC
7	V_mon
8	V_ref
9	GND
10	+3.3V
11	NC
12	GND

Dimensions

Unit	Inch	mm
A	0.192 ± 0.004	4.88 ± 0.10
B	0.120 ± 0.004	3.05 ± 0.10
C	0.230 ± 0.004	5.84 ± 0.10
D	0.140 ± 0.004	3.05 ± 0.10
E	0.795 ± 0.010	3.56 ± 0.25
F	0.184 ± 0.005	4.67 ± 0.13
g	0.229 ± 0.010	5.82 ± 0.25
H	0.300 ± 0.005	7.62 ± 0.13
L	0.700 ± 0.004	17.78 ± 0.10
m	0.050 ± 0.005	1.27 ± 0.13
P	0.100 ± 0.005	2.54 ± 0.13
W	0.660 ± 0.004	16.76 ± 0.10

MTRX-APP-L01
March 15, 2000

Liang D. Tzeng
Multiplex, Inc.
115 Corporate Blvd.
South Plainfield, NJ 07080
tzeng@multiplexinc.com
(908) 757-8817

Multiplex, Inc.
Photonics for Communications

Application notes for MTRX192L optical receiver and the MTRX192L test board

I. The limiting amplifier

The MTRX192L is a high performance optical receiver module that includes a PIN photo diode, a low noise transimpedance amplifier (TIA), and an output limiting amplifier. As shown schematically in Figure 1, while the TIA requires +3.3V and –2V* supplies, the limiting amplifier is biased with a single –2V supply. The signal output from the TIA is AC coupled to the limiting amplifier. Although the limiting amplifier generates differential outputs, for MTRX192L, one of the outputs (Q-bar) is terminated inside the receiver module. Multiplex is currently developing a version of module package that will bring out both of the differential outputs from the limiting amplifier.

The limiting amplifier is essentially a high speed, high sensitivity digital device that will "quantize" the analog signal coming from the TIA. In general, the TIA is a linear, analog circuit with its output carries both the signal and noise characteristics of the detection subsystem. As illustrated in Figure 2, when using an AGC (automatic gain control circuit) as the post-amplifier following the TIA, the output from the AGC should maintain a similar signal and noise characteristics to that of the output from the TIA. As a consequence, a decision circuit is therefore needed to "regenerate" a well defined "1" or "0" binary data stream.

When a limiting amplifier, such as the one incorporated inside the MTRX192L, is used as the post-amplifier, there is, however, a subtle difference in the data regenerating process of the receiver subsystem. Statistically, there are always noise distributions associated with the output from the TIA, for both data level of "1" and "0". Since the limiting amplifier is a "quantizer" (or

* The TIA is designed with the nominal supply voltage of +3.3V and –2V. However, for the current samples, there is a slight mis-calculation in the diode voltage drop inside the TIA IC. As a consequence, the TIA performance will degrade when the negative supply voltage is higher than –1.9V. Therefore, we are asking customers to use –2.2V (± 10%) for evaluation purpose. We will correct this problem before the 2nd quarter of 2000.

a “comparator”), the output from the limiting amplifier is always at a well-defined level of “1” or “0”. It is obvious that the data regenerating “decision” process would have to have occurred inside the limiting amplifier. Therefore, such a limiting amplifier is equivalent to a un-clock decision circuit.

Having accept this “quantization” effect of the limiting amplifier, one would have to pay close attention to the stability issue of the “input reference voltage” (*V_ref*), upon which the limiting amplifier will eventually “decide” whether the input data is “1” or “0”. Needless to say, this input reference voltage stability is especially important at small signal conditions, such as during the BER measurement process. Changes in the system’s operating conditions, such as the power supply voltage variations, operating temperature variations, etc. will affect the optimum *V_ref* value. To minimize the effect associated with the variation of this input voltage reference, we have incorporated a feedback control circuit in the MTRX192L test board.

II. Feed-back control through V_mon and V_ref

The limiting amplifier is designed with DCFL (direct couple FET logic) circuit topology. Changing the *V_ref* value will, in general, affect the output eye crossing level (or, equivalently affect the output duty-cycle). This phenomenon can be utilized to generate a monitoring signal (*V_mon*) at the output of the limiting amplifier. The task then is to keep this *V_mon* to a pre-determined value (*V_set*) by adjusting the *V_ref* value through an analog feedback loop (as illustrated in Figure 1.)

For MTRX192L, the *V_mon* monitoring signal is generated by integrating the unused output port of the limiting amplifier. In this way, small changes in the output pulse shape can be detected easily. There are, however, drawbacks in generating the monitoring signal using the output from the limiting amplifiers. For example, the variation in the supply voltage of the limiting amplifier (-2V) and the operating temperature will both have some effects on the output signal pulse height (peak-to-peak level). Therefore, a certain degree of compensation on this monitoring signal is needed.

Figure 3 schematically shows a simple feedback control circuit, which is included in the MTRX192L test board and consists of mainly a quad operational amplifier and a temperature sensor. The operation of this circuit can be briefly described as following:

Q2 generates the power supply correction factor for the monitoring signal. This correction factor is then added to a pre-determined voltage value (*V_set*) at Q3. The *V_set* can be generated

either digitally through a D/A converter on the system circuit board, or, as indicated in the inset (a) of Figure 3, through a linear variable resistor. On the MTRX192L test board, this variable resistor is mounted on the top surface of the test board. The *V_set* value can be measured by probing on the test board as indicated in Figure 4.

The main purpose of Q3 is to generate the "appropriate" comparison voltage for *V_mon* by taking into account both the power supply correction factor and the temperature correction factor. In the MTRX192L test board, the temperature correction factor is generated through a temperature sensor (National semiconductor LM61 with an output scale factor of 10mV/^{o}C), as shown in the inset (b) of Figure 3. The *V_mon* value from the receiver module is re-calculated in Q1 by referencing to the supply voltage of the limiting amplifier. Finally, Q4 compares this re-calculated *V_mon* value to the corrected *V_set* value and generates an output for the input reference voltage, *V_ref*, to the limiting amplifier.

III. MTRX192L test board

The MTRX192L test board is fabricated for the purpose of evaluation and testing of the MTRX192L receivers. The needed power supplies (+5V, +3.3V and –2V) are fed through the EMI filters as illustrated in Figure 4. The receiver pins are mounted on a pair of clamp fixtures (the first pair of clamp pins toward the fiber pig-tail direction is not used.) A linear variable resistor (10kΩ, multi-turns) is mounted on the top of the test board for the adjustment of the *V_set* value. Upon shipment, this variable resistor has been adjusted to a nominal position. Users may adjust this *V_set* value to optimize the BER performance.

This adjustable *V_set* configuration is similar to the traditional adjustable decision threshold and can be very useful in systems (such as DWDM systems) where different communication channels come with different noise and pulse shape characteristics. When the *V_set* value is generated with the system firmware, the receiver sensitivity for each channel can be individually optimized through the system software interface.

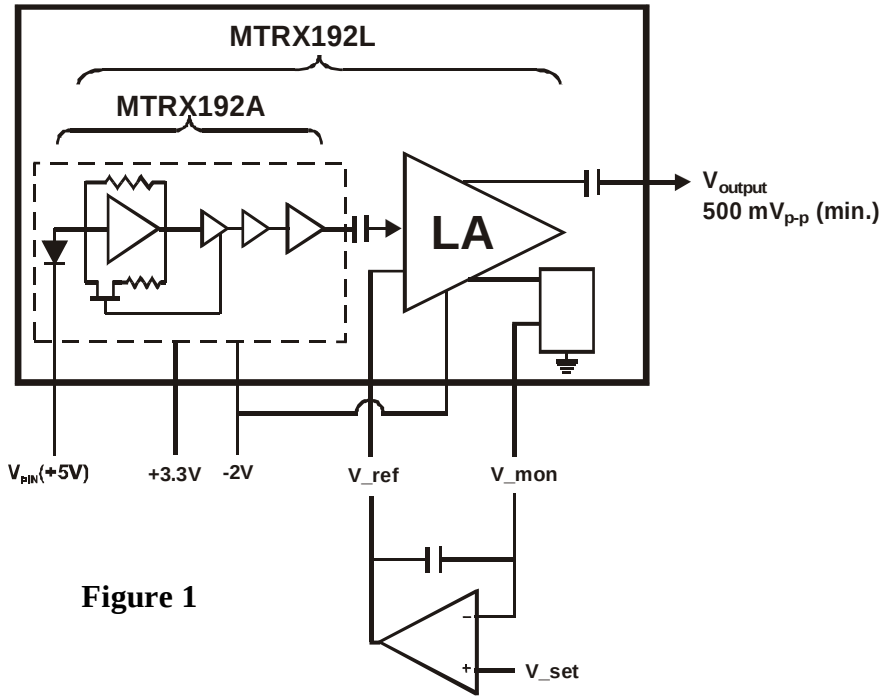


Figure 1

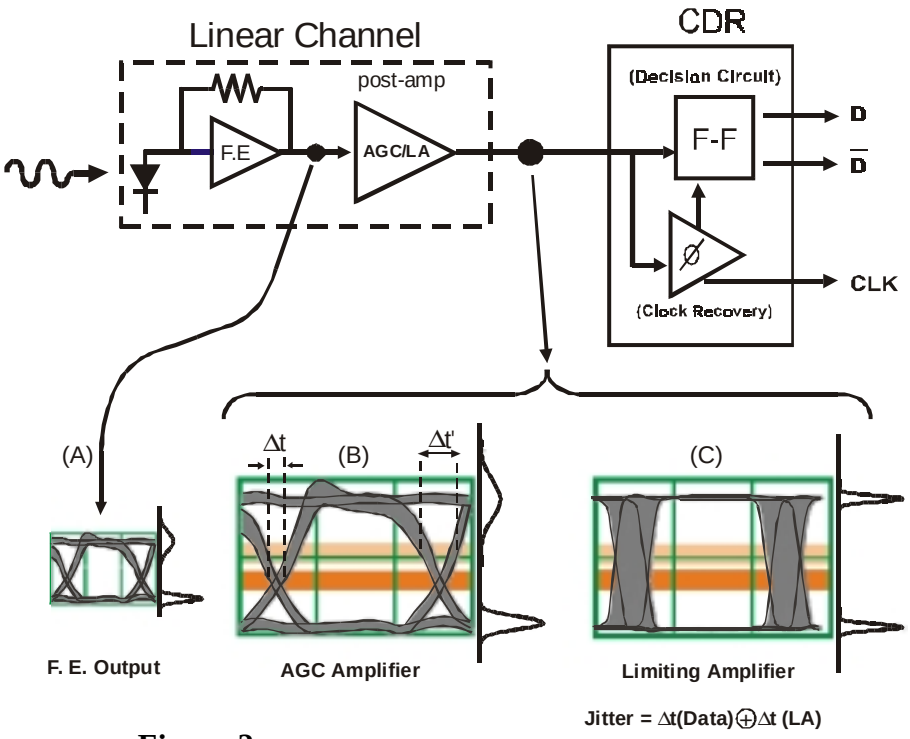


Figure 2

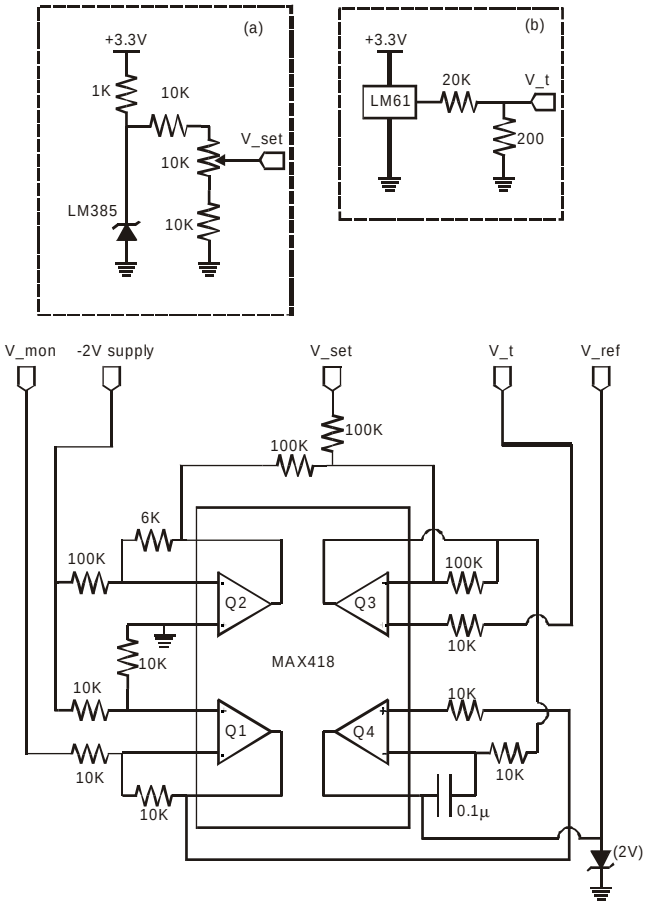


Figure 3

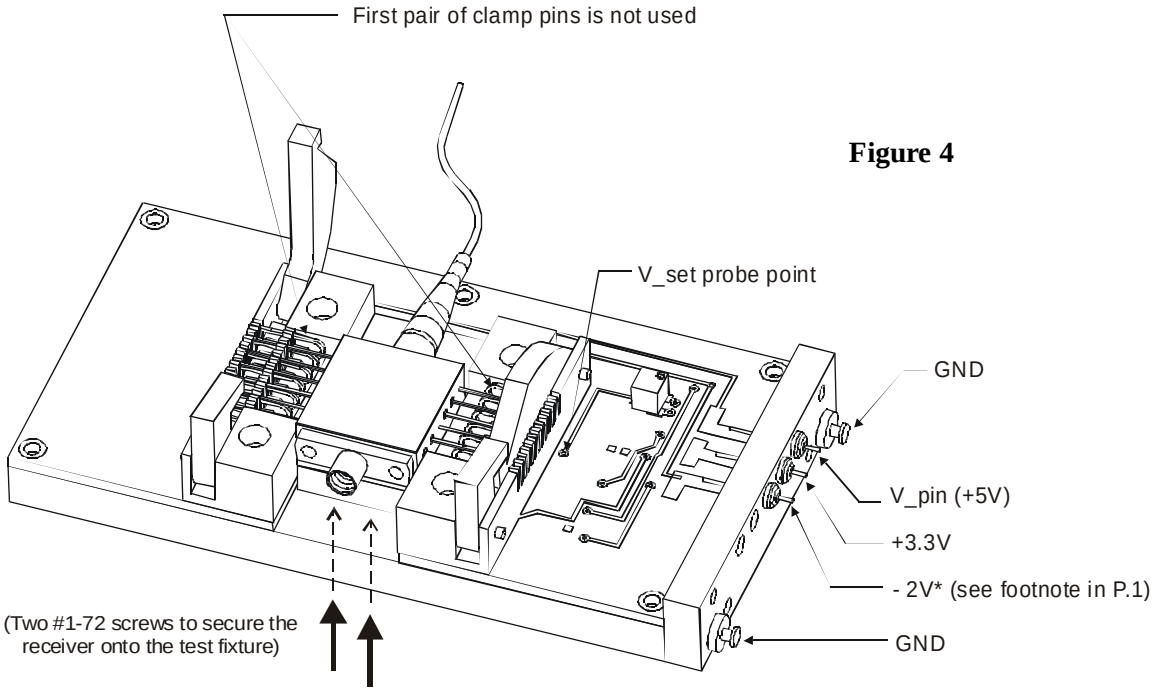


Figure 4

PT4220 Series—48V

EXCALIBUR

Power Trends Products from Texas Instruments

10 Watt Low-Profile 48V Input Isolated DC-DC Converter

SLTS127

(Preliminary 1/17/2001)

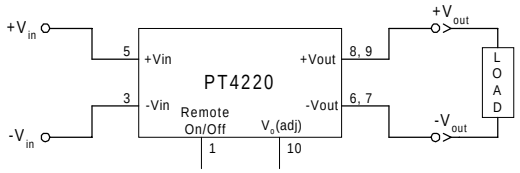
Features

- 10W Output Power
- Input Voltage: 36V to 75V
- 1500 VDC Isolation
- Temp Range: –40°C to +85°C
- Remote On/Off Control
- Adjustable Output Voltage
- Undervoltage Lockout
- Current Limit
- Short-Circuit Protection
- Low-Profile Package (8mm)
- Solderable Copper Case

Description

Power Trends' PT4220 is a new series of isolated DC-DC Converters housed in an ultra-low profile (8mm) solderable copper case. They employ a state-of-the-art high frequency switch mode topology, and are available in either a through-hole or surface-mount package. They are designed for Telecom, Datacom, Industrial, Computer, Medical, and other distributed power applications requiring input-to-output isolation over an industrial temperature range.

Standard Application



PT Series Suffix (PT12345X)

Case/Pin Configuration	
Vertical Through-Hole	N
Horizontal Through-Hole	A
Horizontal Surface Mount	C

(For dimensions and PC board layout, see Package Styles 1520 and 1530.)

Ordering Information

PT4221❒	=1.8 Volts
PT4222❒	=3.3 Volts
PT4223❒	=5.0 Volts
PT4224❒	=12.0 Volts
PT4225❒	=2.5 Volts
PT4226❒	=1.5 Volts

Specifications

Characteristics (T_a=25°C unless noted)	Symbols	Conditions		PT4220 SERIES Min	Typ	Max	Units
Output Current	I_o	Over V_{in} range	$V_o \le 3.3V$ $V_o = 5.0V$ $V_o = 12V$	0.1 (1) 0.1 (1) 0.1 (1)	— — —	3.0 2.0 0.85	A
Short Circuit Current	I_{sc}	V_{in} = 48V	$V_o \le 3.3V$ $V_o = 5.0V$ $V_o = 12.0V$	— — —	5.0 4.0 2.0	— — —	A
Input Voltage Range	V_{in}	I_o = 0.1 to $I_o$max		36.0	48.0	75.0	V
Set-Point Tolerance	V_o tol	V_{in} =48V, I_o =$I_o$max		—	±1.0	±2.0	%V_o
Line Regulation	Reg_{line}	Over V_{in} range @ max I_o		—	±1	±15	mV
Load Regulation	Reg_{load}	10% to 100% of I_o max		—	±5	±20	mV
V_o Temperature Variation	Reg_{temp}	V_{in} =48V, I_o =$I_o$max –40°C ≤ Ta ≤ +85°C		—	±0.3	—	%V_o
V_o Ripple/Noise	V_n	V_{in}=48V, I_o= $I_o$max	$V_o \le 5V$ V_o =12V	— —	50 100	— —	mV_{pp}
Transient Response (no output capacitor)	t_{tr}	50% load change V_o over/undershoot	 $V_o \le 5V$ V_o=12V	— — —	75 150 250	— — —	µSec mV mV
Efficiency	η	V_{in}=48V, I_o =$I_o$max	V_o = 1.5V V_o = 1.8V V_o = 2.5V V_o = 3.3V V_o = 5.0V V_o=12.0V	— — — — — —	71 73 78 81 85 87	— — — — — —	%
Switching Frequency	f_o	Over V_{in} and I_o		250	300	350	kHz
Maximum Operating Temperature Range	T_a	Over V_{in} range		-40	—	+85 (2)	°C
Storage Temperature	T_s	—		-40	—	110	°C
Reliability	MTBF	Per Bellcore TR-332 50% Stress, 40°C, ground benign		4.7	—	—	10^6 Hrs
Mechanical Shock	—	Per Mil-STD-202F, Method 213B, 6mS, Half-sine, mounted to a PCB		—	TBD	—	G's
Mechanical Vibration	—	Per Mil-STD-202F, Method 204D, 10-500Hz, Soldered in a PCB		—	TBD	—	G's
Weight	—			—	20	—	grams
Isolation Capacitance Resistance	— — —	Input–output/Input–case		1500 — 10	— 1100 —	— — —	V pF MΩ
Flammability	—	Materials meet UL 94V-0					
Remote On/Off	On (3) Off	Referenced to $-V_{in}$		4.5 —	— —	— 0.8	V

Pin-Out Information

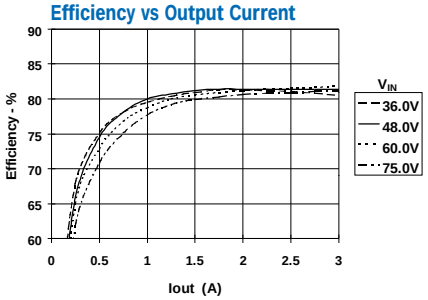
Pin	Function
1	Remote ON/OFF
2	Do not connect
3	$-V_{in}$
4	Do not connect
5	$+V_{in}$
6	$-V_{out}$
7	$-V_{out}$
8	$+V_{out}$
9	$+V_{out}$
10	V_{out} adjust

Notes: *(1) The converter will operate down to no load with reduced specifications.*
(2) See SOA curves or contact the factory for appropriate derating.
(3) Pin 1 has an internal pull-up and may be driven from an open-collector device. If left open, the converter will operate when input power is applied. The maximum voltage that may be applied to Pin 1 is 20V.

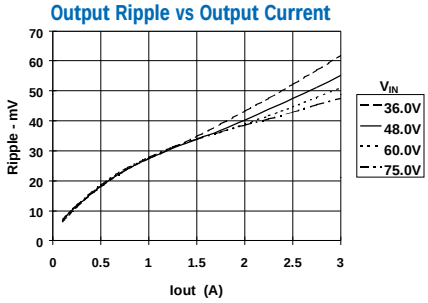
Typical Characteristics

PT4222, V_O =3.3VDC (See Note A)

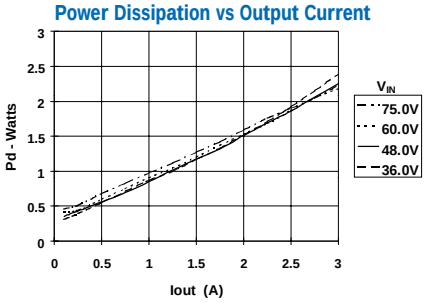
Efficiency vs Output Current



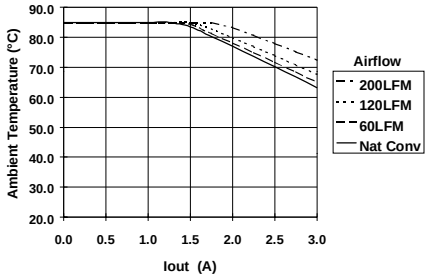
Output Ripple vs Output Current



Power Dissipation vs Output Current

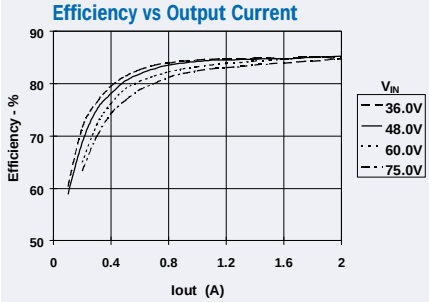


Safe Operating Area @Vin =48V (Note B)

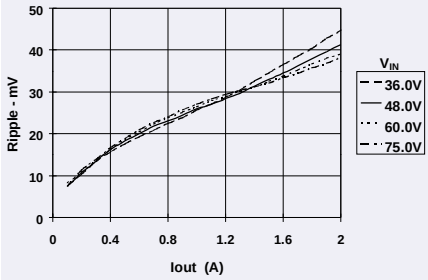


PT4223, V_O =5.0VDC (See Note A)

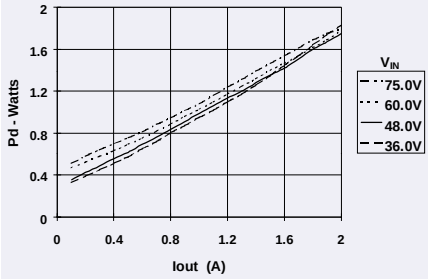
Efficiency vs Output Current



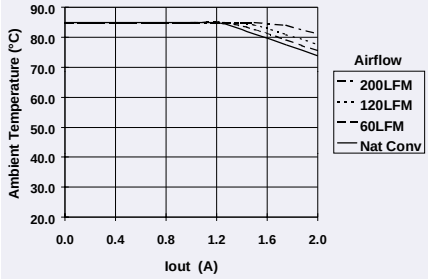
Output Ripple vs Output Current



Power Dissipation vs Output Current

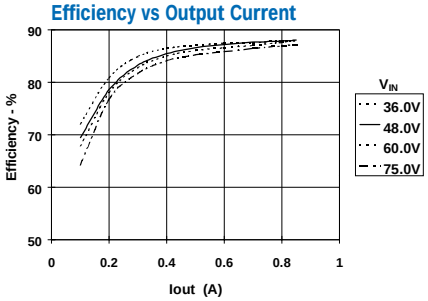


Safe Operating Area @Vin =48V (Note B)

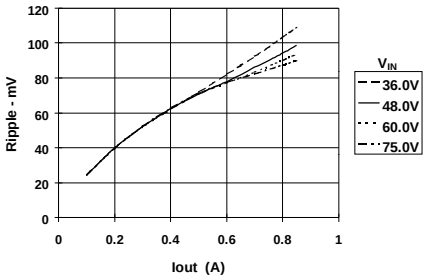


PT4224, V_O =12.0VDC (See Note A)

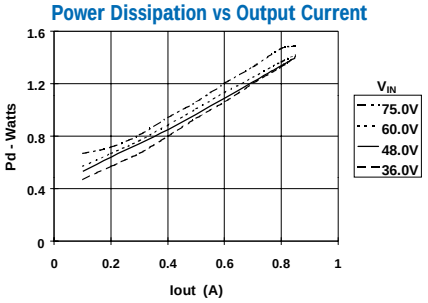
Efficiency vs Output Current



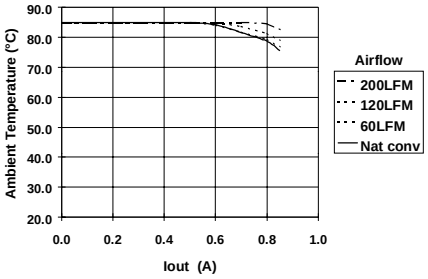
Output Ripple vs Output Current



Power Dissipation vs Output Current



Safe Operating Area @Vin =48V (Note B)



Note A: *All Characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.*

Adjusting the Output Voltage of the 10W Excalibur™ Series of Isolated DC-DC Converters

The factory pre-set output voltage of Power Trends' 10W Excalibur series of isolated DC-DC converters may be adjusted over a narrow range. This is accomplished with the addition of a single external resistor. For the input voltage range specified in the data sheet, Table 1 gives the allowable adjustment range for each model as V_o (min) and V_o (max).

Adjust Up: An increase in the output voltage is obtained by adding a resistor, R_2 between pin 10 (V_o adjust), and pins 6 & 7 ($-V_{out}$).

Adjust Down: Add a resistor (R_1), between pin 10 (V_o adjust) and pins 8 & 9 ($+V_{out}$).

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor, (R_1) or R_2.

Notes:

1. Use only a single 1% resistor in either the (R_1) or R_2 location. Place the resistor as close to the ISR as possible.
2. Never connect capacitors to V_o adjust. Any capacitance added to the V_o adjust control pin will affect the stability of the ISR. The values of (R_1) [adjust down], and R_2 [adjust up], can also be calculated using the following formulas.

$$(R_1) = \frac{56.2\,(V_a - 1.225)}{V_o - V_a} - R_s \quad k\Omega$$

$$R_2 = \frac{68.845}{V_a - V_o} - R_s \quad k\Omega$$

Where, V_o = Original output voltage
V_a = Adjusted output voltage
R_s = Series resistance (Table 1)

Table 1

DC-DC CONVERTER ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt #						
24V Bus	**PT4246**	**PT4241**	**PT4245**	**PT4242**	**PT4243**	**PT4244**
48V Bus	**PT4226**	**PT4221**	**PT4225**	**PT4222**	**PT4223**	**PT4224**
V_o(nom)	1.5V	1.8V	2.5V	3.3V	5.0V	12.0V
Vo(min)	1.45V	1.7V	2.25V	2.95V	4.5V	10.8V
Vo(max)	1.65V	1.98V	2.75V	3.65V	5.5V	13.2V
R_S (kΩ)	243.0	243.0	187.0	187.0	110.0	49.9

Figure 1

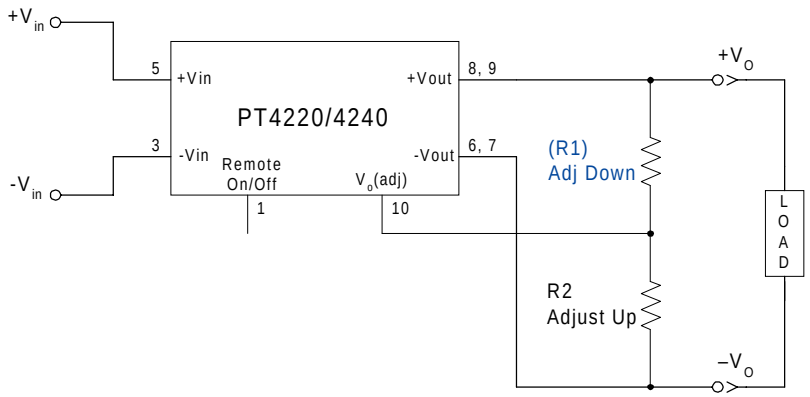


Table 2

DC-DC CONVERTER ADJUSTMENT RESISTOR VALUES

Series Pt #						
24V Bus	**PT4246**	**PT4241**	**PT4245**	**PT4242**	**PT4243**	**PT4244**
48V Bus	**PT4226**	**PT4221**	**PT4225**	**PT4222**	**PT4223**	**PT4224**
V_O(nom)	1.5V	1.8V	2.5V	3.3V	5.0V	12.0V
V_a(req'd)					**V_a(req'd)**	
1.45	(9.9)kΩ				4.5	(258.0)kΩ
1.5					4.6	(364.0)kΩ
1.55	1130.0kΩ				4.7	(541.0)kΩ
1.6	445.0kΩ				4.8	(895.0)kΩ
1.65	216.0kΩ				4.9	(1960.0)kΩ
1.7		(23.9)kΩ			5.0	
1.75		(347.0)kΩ			5.1	578.0kΩ
1.8					5.2	234.0kΩ
1.85		1130.0kΩ			5.3	119.0kΩ
1.9		445.0kΩ			5.4	62.1kΩ
1.95		216.0kΩ			5.5	27.7kΩ
2.25			(43.4)kΩ		10.8	(399.0)kΩ
2.3			(115.0)kΩ		11.0	(499.0)kΩ
2.35			(235.0)kΩ		11.5	(1110.0)kΩ
2.4			(473.0)kΩ		12.0	
2.45			(1190.0)kΩ		12.5	87.8kΩ
2.5					13.0	18.9kΩ
2.55			1190.0kΩ		13.2	7.5kΩ
2.6			501.0kΩ			
2.65			272.0kΩ			
2.7			157.0kΩ			
2.75			88.4kΩ			
2.95				(90.0)kΩ		
3.0				(146.0)kΩ		
3.05				(223.0)kΩ		
3.1				(340.0)kΩ		
3.15				(534.0)kΩ		
3.2				(923.0)kΩ		
3.25				(2090.0)kΩ		
3.3						
3.35				1190.0kΩ		
3.4				501.0kΩ		
3.45				272.0kΩ		
3.5				157.0kΩ		
3.55				88.4kΩ		
3.6				42.5kΩ		
3.65				9.7kΩ		

R1 = (Blue) R2 = Black

Using the Inhibit Function on the PT4220/4240 Isolated 10W Excalibur™ DC/DC Converters

Applications requiring output voltage On/Off control, the PT4220/4240 DC/DC converter series incorporates a "*Remote On/Off*" control (pin 1). This feature can be used when there is a requirement for the module to be switched off without removing the applied input source voltage.

The converter functions normally with Pin 1 open-circuit, providing a regulated output voltage when a valid source voltage is applied to $+V_{in}$ (pin 5), with respect to $-V_{in}$ (pin 3). When a low-level [1] ground signal is applied to pin 1, the converter output will be turned off.

Figure 1 shows an application schematic, which details the typical use of the *Remote On/Off* function. Note the discrete transistor (Q1). The control pin has its own internal pull-up, allowing the pin to be controlled with an open-collector or open-drain device (See notes 2 & 3). Table 1 gives the threshold requirements.

When placed in the "Off" state, the standby current drawn from the input source is typically reduced to less than 1mA.

Table 1; Pin 1 Remote On/Off Control Parameters [1]

Parameter	Min	Typ	Max
Enable (V_{IH})	4.5V	—	—
Disable (V_{IL})	—	—	0.8V
Von [Open-Circuit]		5.0V	
Ioff [pin 1 at $-V_{in}$]	—	—	–0.5mA

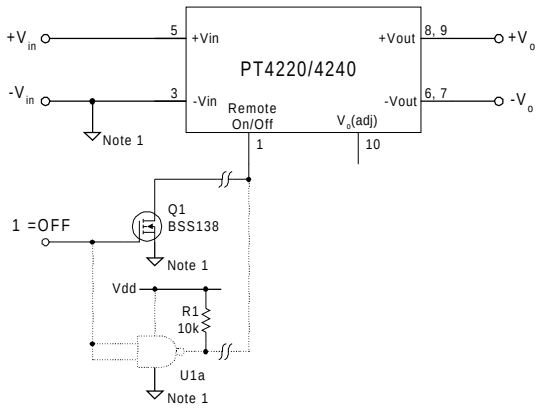
Notes:

1. The *Remote On/Off* control uses $-V_{in}$ (pin 3) as its ground reference. All voltages specified are with respect to $-V_{in}$.
2. Use an open-collector device (preferably a discrete transistor) for the *Remote On/Off* input. A pull-up resistor is not necessary. To disable the output voltage, the control pin should be pulled low to less than +0.8VDC.
3. The *Remote On/Off* pin may be controlled with devices that have a totem-pole output. This is provided the drive voltage meets the threshold requirements in Table 1. *Do not* apply more than +20V. If a TTL gate is used, a pull-up resistor may be required to the logic supply voltage.
4. The PT4220/4240 converters incorporate an "Under-Voltage Lockout" (UVLO). The UVLO will override pin 1, and keep the module off when the input voltage to the converter is low. Table 2 gives the UVLO input voltage thresholds.

Table 2; UVLO Thresholds [4]

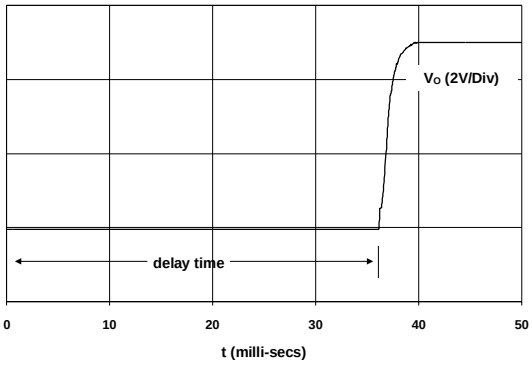
Series	V_{in} Range	UVLO Threshold
PT4220	36 – 75V	32V ±2V
PT4240	18 – 36V	TBD

Figure 1



Turn-On Time: In the circuit of Figure 1, turning Q_1 on applies a low-voltage to pin 1 and disables the converter output. Correspondingly, turning Q_1 off allows pin 1 to be pulled high by an internal pull-up resistor. The converter produces a regulated output voltage within 60 milli-secs. Although the rise-time of the output is short (<5ms), the delay time will vary between 0 and 55ms depending upon the input voltage and the module's internal timing. Figure 2 shows shows an example of the output response for a PT4223 (5.0V), following the turn-off of Q_1 at time t =0. The waveform was measured with a 48Vdc input voltage, and 3.3Ω resistive load.

Figure 2

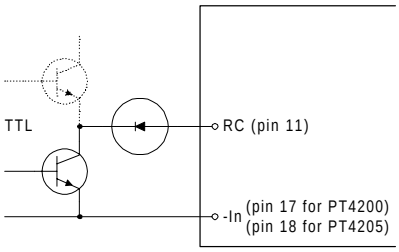


Using the PT4200/4205/4300 DC to DC Converter

Remote Control (RC) Turn-on or turn-off can be realized by using the RC pin. Normal operation is achieved if pin 11 is open. If pin 11 is connected to pin 17 (PT4200/4300) or pin 18 (PT4205), the power module turns off. To insure safe turn-off, the voltage difference between pin 11 and 17 or 18 should be less than 1.0V. RC is compatible with TTL open collector outputs with a sink capacity > 300µA (see figure 28).

Figure 28

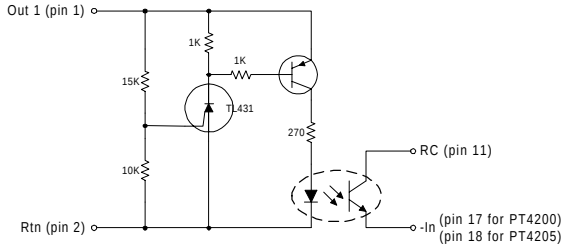
PT4200/4205/4300 REMOTE CONTROL



Over Voltage Protection (OVP) The remote control can also be utilized for OVP by using the external circuitry shown in figure 29. Resistor values are for 5V output applications, but can easily be adjusted for other output voltages and the desired OVP level.

Figure 29

PT4200/4205/4300 OVER VOLTAGE PROTECTION



Turn-on/off Input Voltage The power module monitors the input voltage and will turn on and turn off at predetermined levels set by means of external resistors.

To increase V_{Ion} connect a resistor between pin 11 and 17 (PT4200/4300) or 18 (PT4205) (see figure 30). The resistance is determined by the following equations; (a) PT4200/4300, (b) PT4205:

(a) $R_{Ion} = 100 \times (100.2 - V_{Ion})/(V_{Ion} - 36.5)$ kΩ (for V_{Ion}>37V)

(b) $R_{Ion} = 1000 \times (1110 - V_{Ion})/(V_{Ion} - 18.7)$ kΩ (for V_{Ion}>18.7V)

where 18.7 or 36.5 is the typical unadjusted turn-on input voltage. V_{Ioff} is the adjusted turn-off input voltage and is determined by V_{Ion}-V_{Ioff} = 2V (typical value).

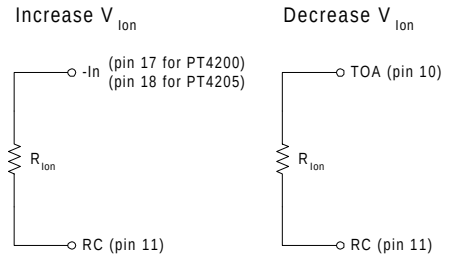
To decrease V_{Ion} connect a resistor between pin 10 and 11 (see figure 30). The resistance is determined by the following equations; (a) PT4200/4300, (b) PT4205:

(a) $R_{Ion} = 364 \times (V_{Ion} - 29.9)/(36.5 - V_{Ion})$ kΩ (for 30<V_{Ion}< 36V)

(b) $R_{Ion} = 25 \times (V_{Ion} - 16.9)/(18.7 - V_{Ion})$ kΩ (for 16.9<V_{Ion}< 18.7V)

Figure 30

PT4200/4205/4300 TURN-ON/OFF INPUT VOLTAGE ADJUSTMENT



Ouput Voltage Adjust (Vadj) Ouput voltage can be adjusted by using an external resistor. Typical adjust range is ±15%. If pin 8 and 9 are not connected together, the output will decrease to a low value. To increase V_O, a resistor should be connected between pin 8/9 and 18. To decrease V_O, a resistor should be connected between pin 8 and 9 (see figure 31).

The typical resistor value to **increase** V_O is determined by:

$$R_{adj} = k_1 \times (k_2 - V_O)/(V_O - V_{Oi}) \text{ kΩ}$$

where: V_O is the desired output voltage

V_{Oi} is the typical output voltage initial setting

and	k_1=0.684	k_2=2.46V	PT4201
	k_1=0.495	k_2=3.93V	PT4202
	k_1=0.495	k_2=5.87V	PT4203
	k_1=0.566	k_2=15.00V	PT4204*
	k_1=3.180	k_2=3.78V	PT4205
	k_1=3.180	k_2=5.85V	PT4206
	k_1=0.495	k_2=5.82V	PT4301
	k_1=0.495	k_2=3.93V	PT4302
	k_1=0.566	k_2=15.00V	PT4303*

The typical resistor value to **decrease** V_O is determined by:

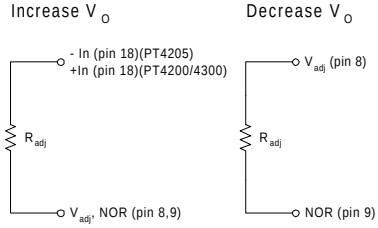
$$R_{adj} = k_1 \times (V_{Oi} - V_O)/(V_O - k_2) \text{ kΩ}$$

where	k_1=2.751	k_2=1.75V	PT4201
	k_1=1.986	k_2=2.59V	PT4202
	k_1=1.986	k_2=4.12V	PT4203
	k_1=2.284	k_2=9.52V	PT4204
	k_1=17.2	k_2=1.70V	PT4205
	k_1=12.5	k_2=4.28V	PT4206
	k_1=1.986	k_2=4.12V	PT4301
	k_1=1.986	k_2=2.59V	PT4302
	k_1=2.284	k_2=9.52V	PT4303

* Over 13.8V output voltage, the input voltage range is limited to 38-65V.

Figure 31

PT4200/4205/4300 OUTPUT VOLTAGE ADJUSTMENT



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

MC78L00A Series

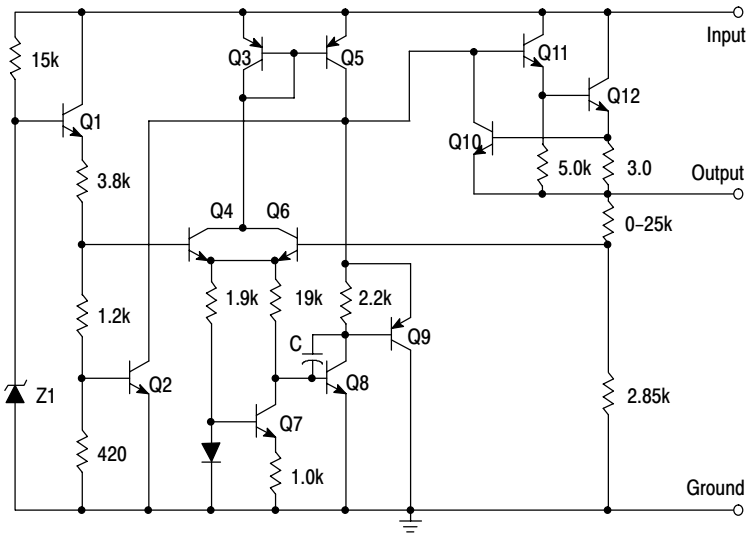
Three-Terminal Low Current Positive Voltage Regulators

The MC78L00A Series of positive voltage regulators are inexpensive, easy–to–use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

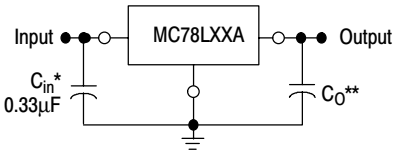
These devices offer a substantial performance advantage over the traditional zener diode–resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00A Series)

Representative Schematic Diagram



Standard Application



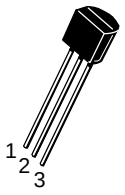
A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

*C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O is not needed for stability; however, it does improve transient response.

ON Semiconductor™

http://onsemi.com



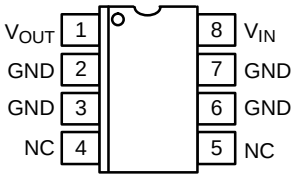
TO–92
P SUFFIX
CASE 029

Pin: 1. Output
2. Ground
3. Input

SOP–8*
D SUFFIX
CASE 751

*SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

MAXIMUM RATINGS (T_A = +125°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L05AC, AB			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	 – –	 55 45	 150 100	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 11 5.0	 60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 4.75 4.75	 – –	 5.25 5.25	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.8 –	 6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L08AC, AB			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	 – –	 20 12	 175 125	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 7.6 7.6	 – –	 8.4 8.4	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L09AC, AB			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 11.5 Vdc ≤ V_I ≤ 24 Vdc 12 Vdc ≤ V_I ≤ 24 Vdc	Reg_{line}	 – –	 20 12	 175 125	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 15 8.0	 90 40	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 8.5 8.5	 – –	 9.5 9.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.0 –	 6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L12AC, AB			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 14.5 Vdc ≤ V_I ≤ 27 Vdc 16 Vdc ≤ V_I ≤ 27 Vdc	Reg_{line}	 – –	 120 100	 250 200	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 20 10	 100 50	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 11.4 11.4	 – –	 12.6 12.6	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.2 –	 6.5 6.0	mA
Input Bias Current Change (16 Vdc ≤ V_I ≤ 27 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L15AC, AB			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 – –	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 – –	 15.75 15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.4 –	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L18AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 – –	 45 35	 325 275	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 – –	 18.9 18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I ≤ 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L24AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 27.5 Vdc ≤ V_I ≤ 38 Vdc 28 Vdc ≤ V_I ≤ 80 Vdc 27 Vdc ≤ V_I ≤ 38 Vdc	Reg_{line}	 – – –	 – 50 60	 – 300 350	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 40 20	 200 100	mV
Output Voltage (28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (28 Vdc ≤ V_I = 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA) (27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 22.8 22.8	 – –	 25.2 25.2	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (28 Vdc ≤ V_I ≤ 38 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	Vdc

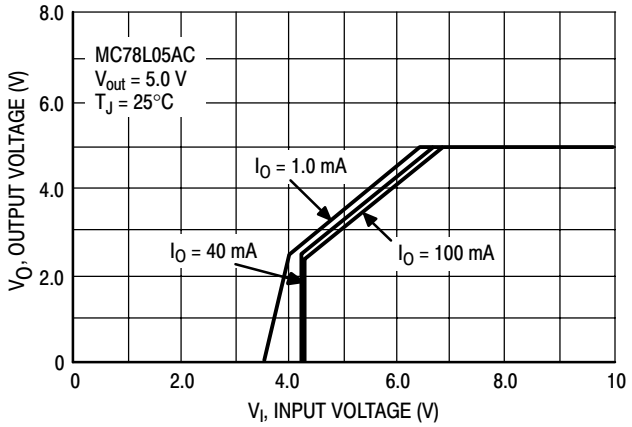


Figure 1. Dropout Characteristics

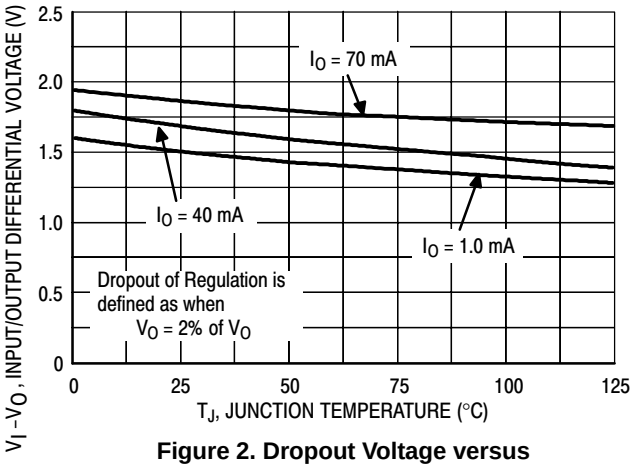


Figure 2. Dropout Voltage versus Junction Temperature

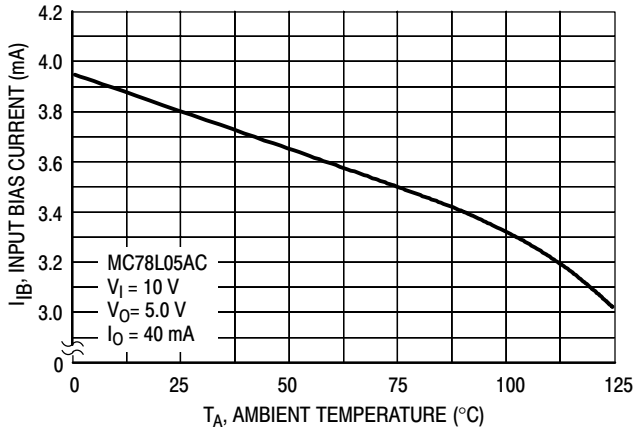


Figure 3. Input Bias Current versus Ambient Temperature

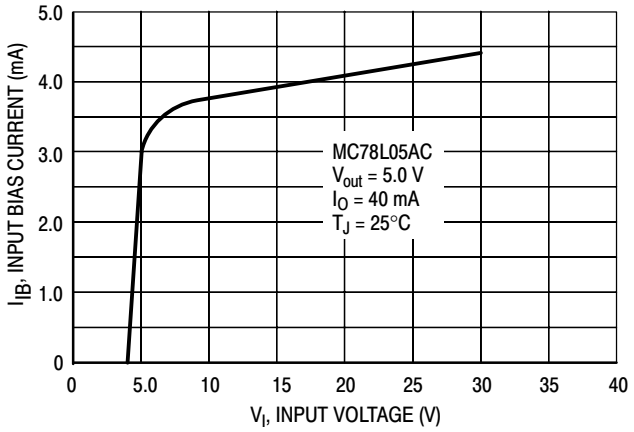


Figure 4. Input Bias Current versus Input Voltage

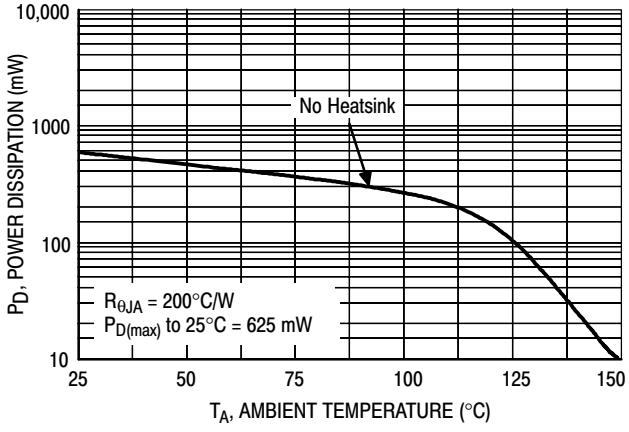


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature – TO–92 Type Package

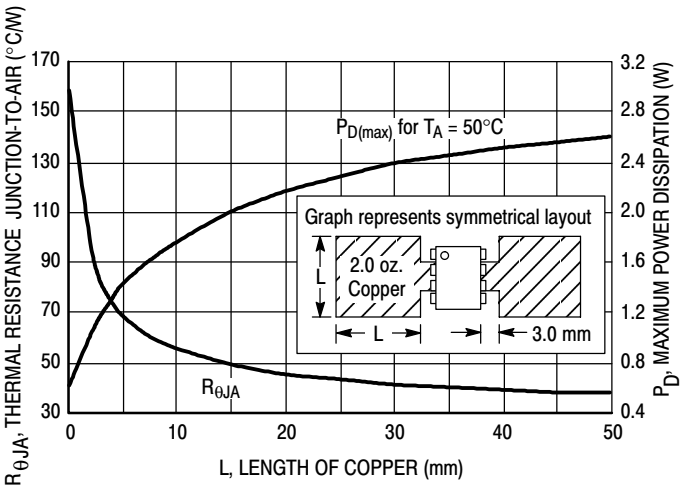


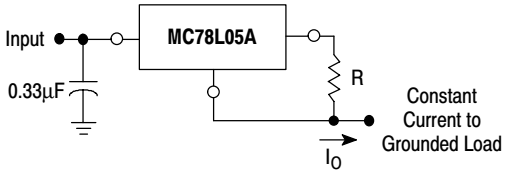
Figure 6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

APPLICATIONS INFORMATION

Design Considerations

The MC78L00A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 7. Current Regulator

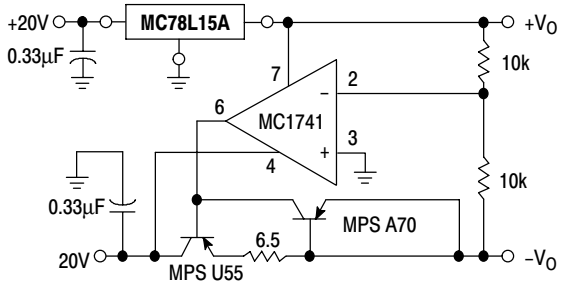


Figure 8. ± 15 V Tracking Voltage Regulator

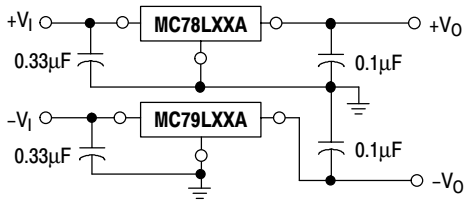


Figure 9. Positive and Negative Regulator

ORDERING INFORMATION

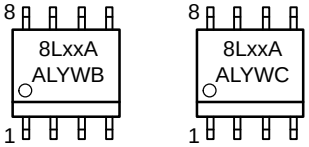
Device	Output Voltage	Operating Temperature Range	Package	Shipping
MC78L05ABD	5.0 V	T_J = –40° to +125°C	SOP–8	98 Units/Rail
MC78L05ABDR2			SOP–8	2500 Tape & Reel
MC78L05ABP			TO–92	2000 Units/Bag
MC78L05ABPRA			TO–92	2000 Tape & Reel
MC78L05ABPRE			TO–92	2000 Units/Bag
MC78L05ABPRM			TO–92	2000 Ammo Pack
MC78L05ACD		T_J = 0° to +125°C	SOP–8	98 Units/Rail
MC78L05ACDR2			SOP–8	2500 Tape & Reel
MC78L05ACP			TO–92	2000 Units/Bag
MC78L05ACPRA			TO–92	2000 Tape & Reel
MC78L05ACPRE			TO–92	2000 Tape & Reel
MC78L05ACPRM			TO–92	2000 Ammo Pack
MC78L05ACPRP			TO–92	2000 Ammo Pack
MC78L08ABD	8.0 V	T_J = –40° to +125°C	SOP–8	98 Units/Rail
MC78L08ABDR2			SOP–8	2500 Tape & Reel
MC78L08ABP			TO–92	2000 Units/Bag
MC78L08ABPRA			TO–92	2000 Tape & Reel
MC78L08ABPRP			TO–92	2000 Units/Bag
MC78L08ACD		T_J = 0° to +125°C	SOP–8	98 Units/Rail
MC78L08ACDR2			SOP–8	2500 Tape & Reel
MC78L08ACP			TO–92	2000 Units/Bag
MC78L08ACPRA			TO–92	2000 Tape & Reel
MC78L08ACPRE			TO–92	2000 Tape & Reel
MC78L08ACPRP			TO–92	2000 Ammo Pack
MC78L09ABD	9.0 V	T_J = –40° to +125°C	SOP–8	98 Units/Rail
MC78L09ABDR2			SOP–8	2500 Tape & Reel
MC78L09ABPRA			TO–92	2000 Units/Bag
MC78L09ABPRP			TO–92	2000 Units/Bag
MC78L09ACD		T_J = 0° to +125°C	SOP–8	98 Units/Rail
MC78L09ACDR2			SOP–8	2500 Tape & Reel
MC78L09ACP			TO–92	2000 Units/Bag

ORDERING INFORMATION (continued)

Device	Output Voltage	Operating Temperature Range	Package	Shipping
MC78L12ABD	12 V	T_J = –40° to +125°C	SOP–8	98 Units/Rail
MC78L12ABDR2			SOP–8	2500 Tape & Reel
MC78L12ABP			TO–92	2000 Units/Bag
MC78L12ABPRP			TO–92	2000 Units/Bag
MC78L12ACD		T_J = 0° to +125°C	SOP–8	98 Units/Rail
MC78L12ACDR2			SOP–8	2500 Tape & Reel
MC78L12ACP			TO–92	2000 Units/Bag
MC78L12ACPRA			TO–92	2000 Tape & Reel
MC78L12ACPRE			TO–92	2000 Tape & Reel
MC78L12ACPRM			TO–92	2000 Ammo Pack
MC78L12ACPRP			TO–92	2000 Ammo Pack
MC78L15ABD	15 V	T_J = –40° to +125°C	SOP–8	98 Units/Rail
MC78L15ABDR2			SOP–8	2500 Tape & Reel
MC78L15ABP			TO–92	2000 Units/Bag
MC78L15ABPRA			TO–92	2000 Tape & Reel
MC78L15ABPRP			TO–92	2000 Units/Bag
MC78L15ACD		T_J = 0° to +125°C	SOP–8	98 Units/Rail
MC78L15ACDR2			SOP–8	2500 Tape & Reel
MC78L15ACP			TO–92	2000 Units/Bag
MC78L15ACPRA			TO–92	2000 Tape & Reel
MC78L15ACPRP			TO–92	2000 Ammo Pack
MC78L18ABP	18 V	T_J = –40° to +125°C	TO–92	2000 Units/Bag
MC78L18ACP		T_J = 0° to +125°C	TO–92	2000 Units/Bag
MC78L18ACPRA			TO–92	2000 Tape & Reel
MC78L18ACPRM			TO–92	2000 Units/Bag
MC78L18ACPRP			TO–92	2000 Ammo Pack
MC78L24ABP	24 V	T_J = –40° to +125°C	TO–92	2000 Units/Bag
MC78L24ACP		T_J = 0° to +125°C	TO–92	2000 Units/Bag
MC78L24ACPRA			TO–92	2000 Tape & Reel
MC78L24ACPRP			TO–92	2000 Ammo Pack

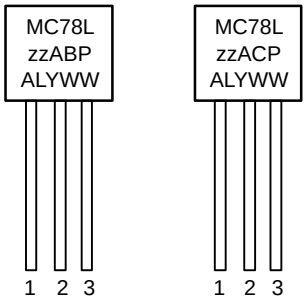
MARKING DIAGRAMS

SOP–8
D SUFFIX
CASE 751



xx = 05, 08, 09, 12, or 15
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
B, C = Temperature Range

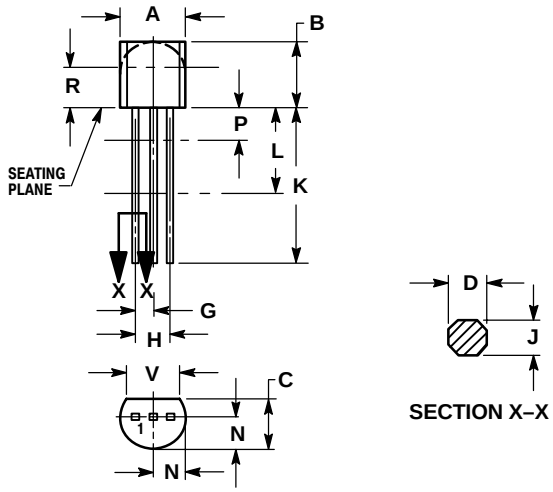
TO–92
P SUFFIX
CASE 029



zz = 05, 08, 09, 12, 15, 18 or 24
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week

PACKAGE DIMENSIONS

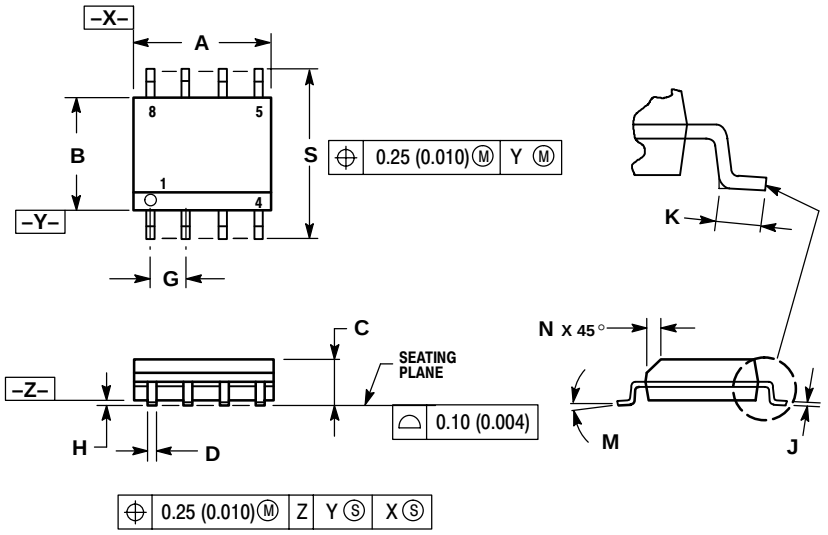
TO–92
P SUFFIX
CASE 29–11
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

SOP–8
D SUFFIX
CASE 751–07
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (Mon–Fri 2:30pm to 7:00pm CET)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (Mon–Fri 2:00pm to 7:00pm CET)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (Mon–Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781
*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com
Toll–Free from Mexico: Dial 01–800–288–2872 for Access – then Dial 866–297–9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.

19-1098; Rev 1; 12/96

MAXIM

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

General Description

The MAX525 combines four low-power, voltage-output, 12-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX525 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset which clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. The DAC registers can be simultaneously updated via the 3-wire serial interface. All logic inputs are TTL/CMOS-logic compatible.

Applications

Industrial Process Controls
Automatic Test Equipment
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems

Features

- ♦ **Four 12-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation**
  10µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **Capable of Recalling Last State Prior to Shutdown**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**

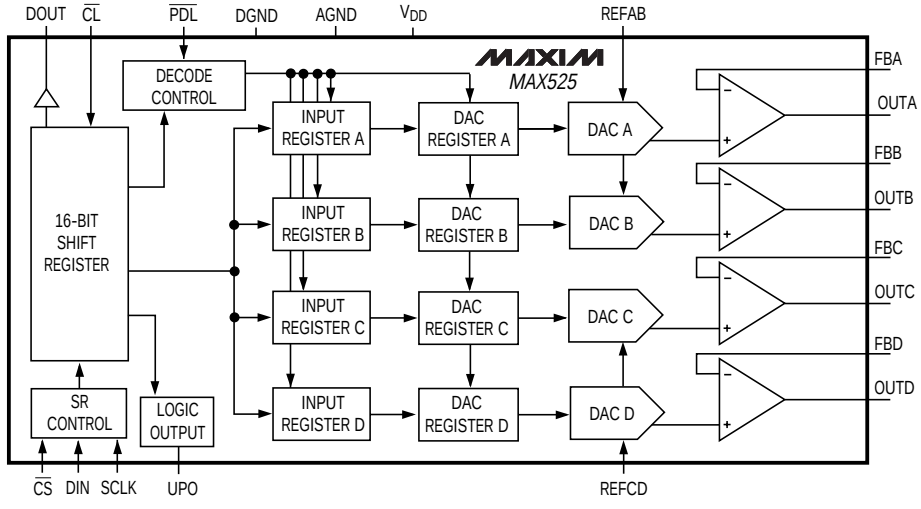
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX525ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX525BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX525ACAP	0°C to +70°C	20 SSOP	±1/2
MAX525BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc. Microwire is a trademark of National Semiconductor Corp.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW

Operating Temperature Ranges
MAX525_C_P .....0°C to +70°C
MAX525_E_P .....-40°C to +85°C
MAX525_MJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX525A		±0.25	±0.5	LSB
		MAX525B			±1.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE			-0.8	±2.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		100	600	µV/V
MATCHING PERFORMANCE (T_A = +25°C)						
Gain Error	GE			-0.8	±2.0	LSB
Offset Error				±1.0	±6.0	mV
Integral Nonlinearity	INL			±0.35	±1.0	LSB
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code-dependent, minimum at code 555 hex	10			kΩ
Reference Current in Shutdown				0.01	±1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		12		µs
Output Voltage Swing		Rail to rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				15		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.85	0.98	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.
Note 2: Accuracy is better than 1.0LSB for V_{OUT} = 6mV to V_{DD} - 60mV, guaranteed by PSR test on end points.
Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

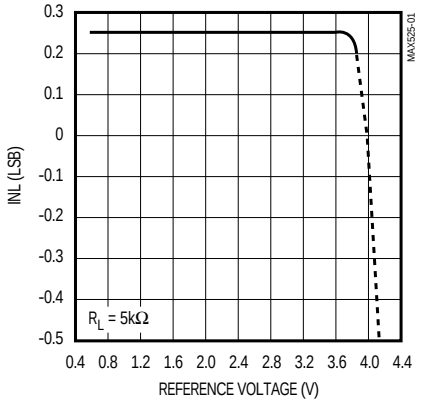
(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

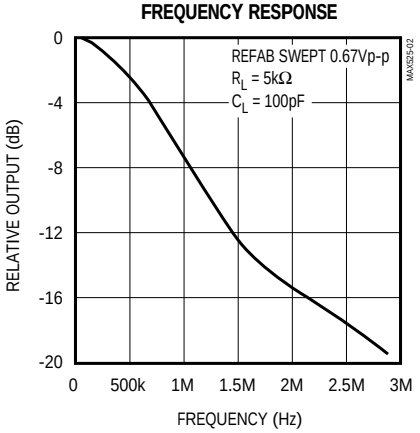
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

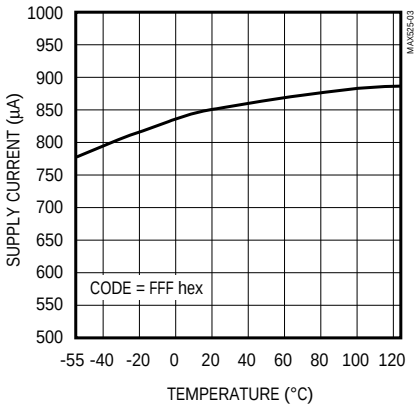
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



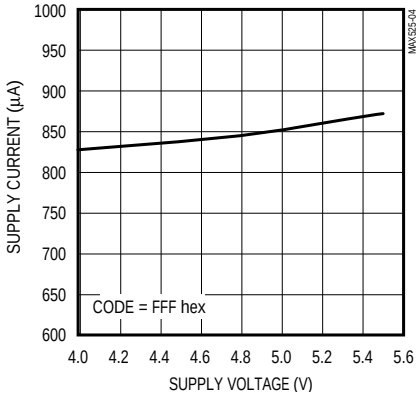
SUPPLY CURRENT vs. TEMPERATURE



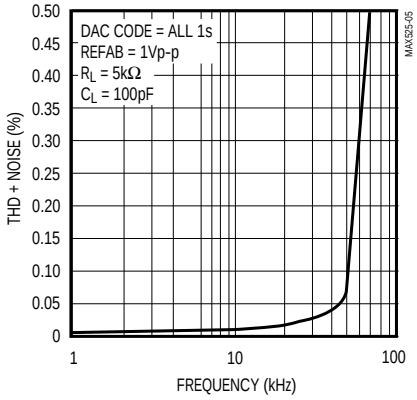
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

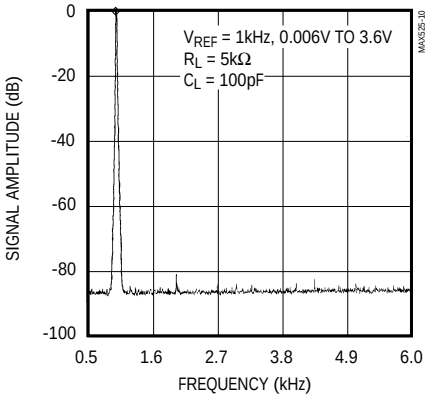
SUPPLY CURRENT vs. SUPPLY VOLTAGE



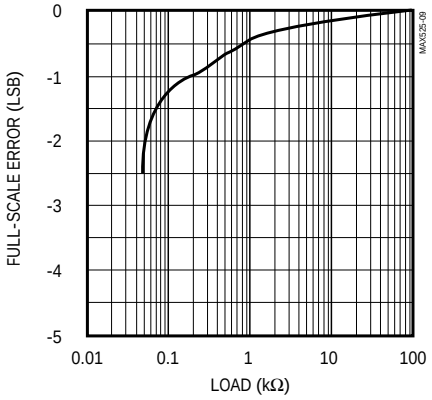
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



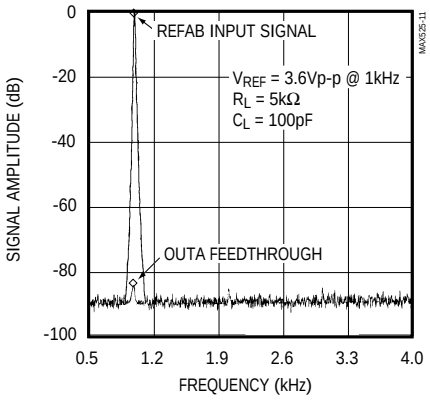
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

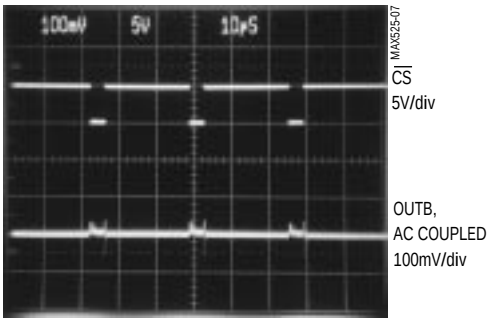


Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

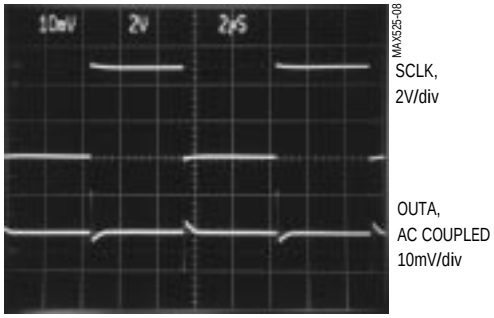
MAJOR-CARRY TRANSITION



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF

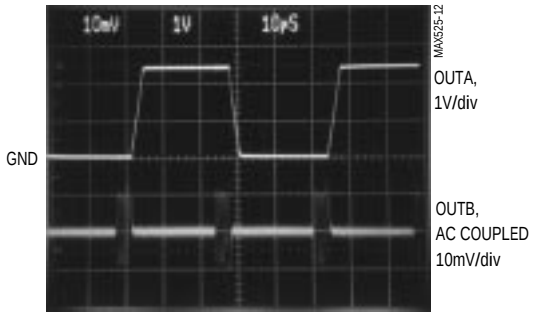
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 5V, DIN = 0V
DAC A CODE SET TO 800 hex

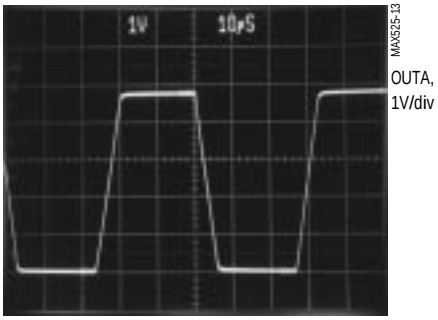
ANALOG CROSSTALK



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
DAC A CODE SWITCHING FROM 00B hex TO FFF hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF
SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clear All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

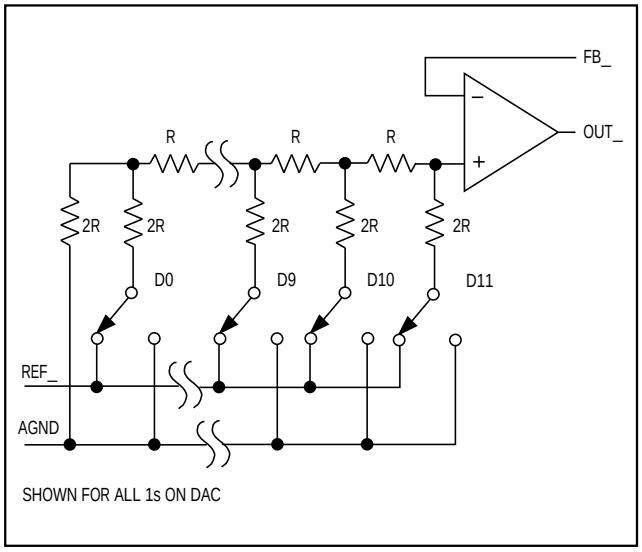


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX525 contains four 12-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT\_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT\_} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code-dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 555 hex, to a high value exceeding several gigohms (leakage currents) with an input code of 000 hex. Because the input impedance at the reference pins is code-dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.025LSB (0.061LSB worst case) when driving both MAX525 reference inputs simultaneously at 2.5V. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX525's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF with an input code of all 1s.

Output Amplifiers

All MAX525 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to the inverting input of each output amplifier provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX525 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX525 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Power-Down Mode

The MAX525 features a software-programmable shutdown that reduces supply current to a typical value of 10µA. The power-down lockout ($\overline{PDL}$) pin must be high to enable the shutdown mode. Writing 1100XXXXXXXXXXX as the input-control word puts the MAX525 in power-down mode (Table 1).

In power-down mode, the MAX525 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in power-down, allowing the MAX525 to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 15µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX525's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 12 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX525's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX525's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX525's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX525 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 12 data bits D11…D0 (Figure 4). The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when coming out of shutdown mode.

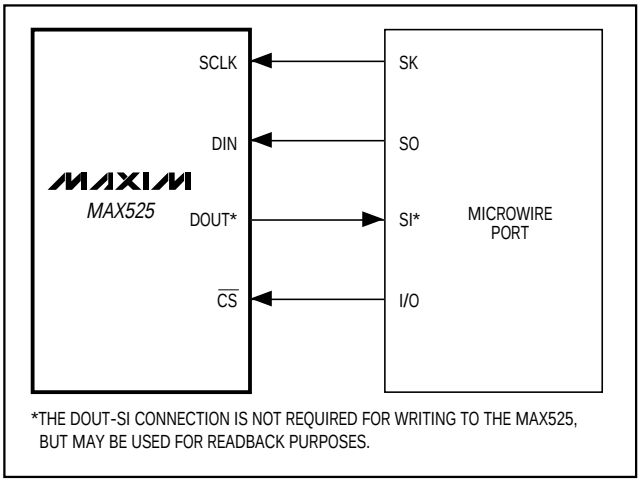


Figure 2. Connections for Microwire

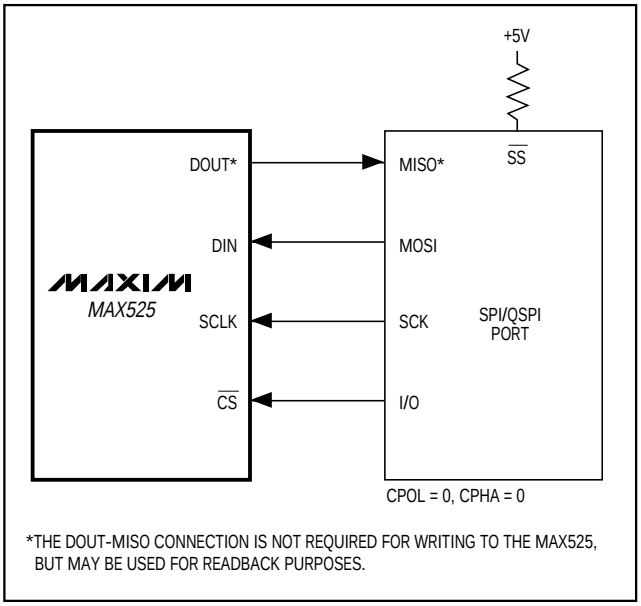


Figure 3. Connections for SPI/QSPI

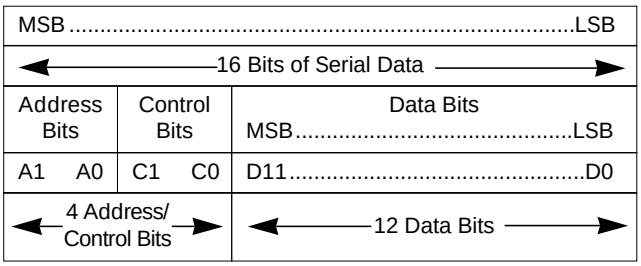


Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
A1	A0	C1	C0	D11.....D0 MSB LSB	
0	0	0	1	12-bit DAC data	Load input register A; DAC registers unchanged.
0	1	0	1	12-bit DAC data	Load input register B; DAC registers unchanged.
1	0	0	1	12-bit DAC data	Load input register C; DAC registers unchanged.
1	1	0	1	12-bit DAC data	Load input register D; DAC registers unchanged.
0	0	1	1	12-bit DAC data	Load input register A; all DAC registers updated.
0	1	1	1	12-bit DAC data	Load input register B; all DAC registers updated.
1	0	1	1	12-bit DAC data	Load input register C; all DAC registers updated.
1	1	1	1	12-bit DAC data	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXXXX	Update all DAC registers from their respective input registers (start-up).
1	0	0	0	12-bit DAC data	Load all DAC registers from shift register (start-up).
1	1	0	0	XXXXXXXXXXXX	Shutdown (provided $\overline{PDL}$ = 1)
0	0	1	0	XXXXXXXXXXXX	UPO goes low (default)
0	1	1	0	XXXXXXXXXXXX	UPO goes high
0	0	0	0	XXXXXXXXXXXX	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXXXX	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXXXX	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX525 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX525 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX525 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire™, SPI™/QSPI™, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX525 serial interface (Table 1).

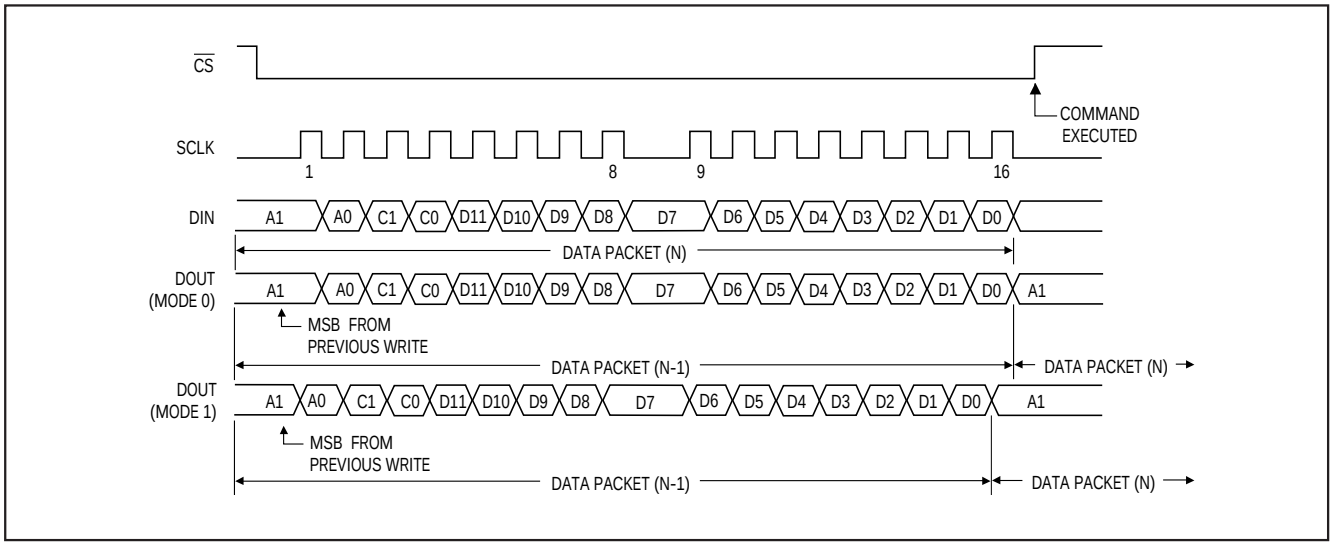


Figure 5. Serial-Interface Timing Diagram

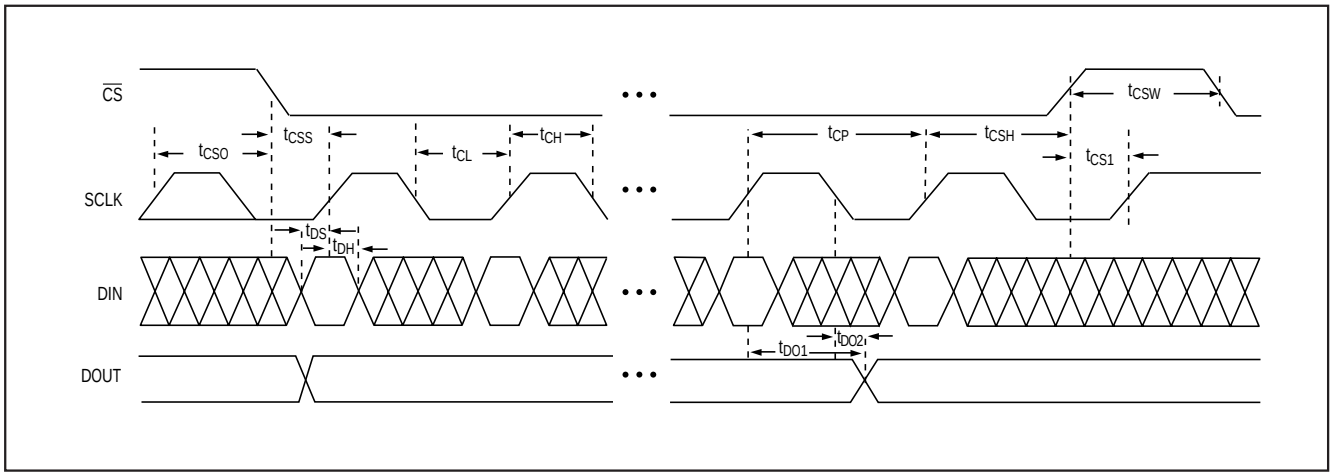


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout (PDL)

The power-down lockout pin PDL disables software shutdown when low. When in shutdown, transitioning PDL from high to low wakes up the part with the output set to the state prior to shutdown. PDL could also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX525s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX525's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics.*

Figure 8 shows an alternate method of connecting several MAX525s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input (CS) is required for each IC.

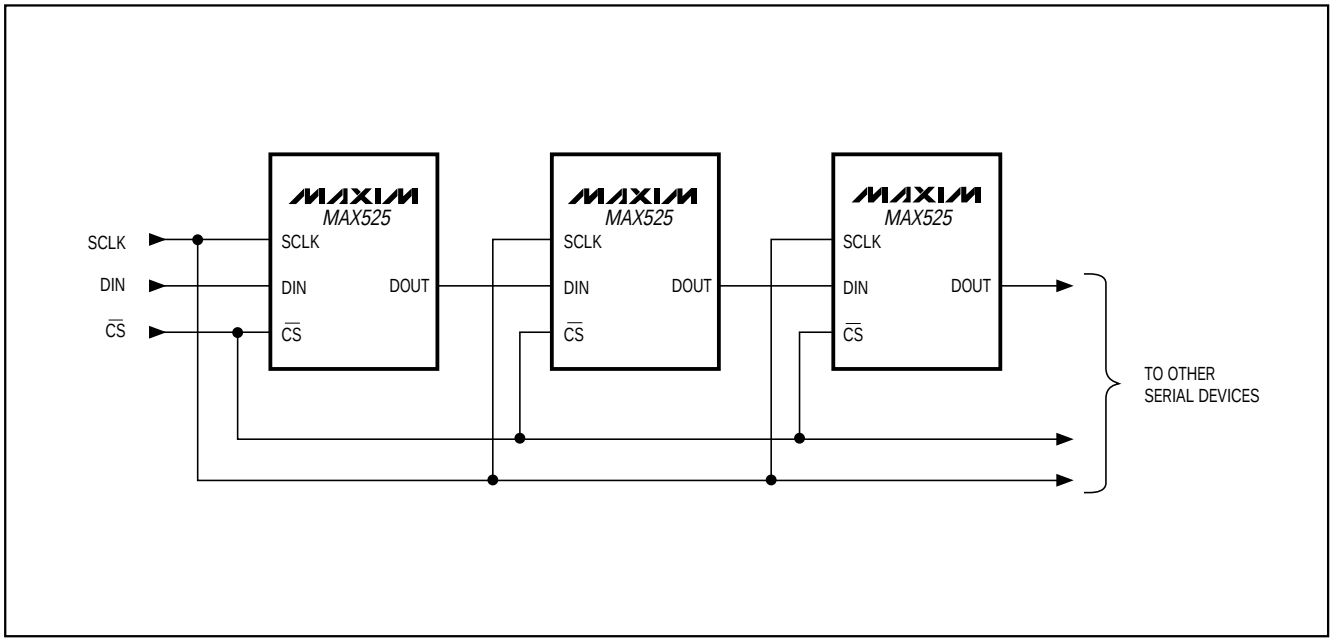


Figure 7. Daisy-Chaining MAX525s

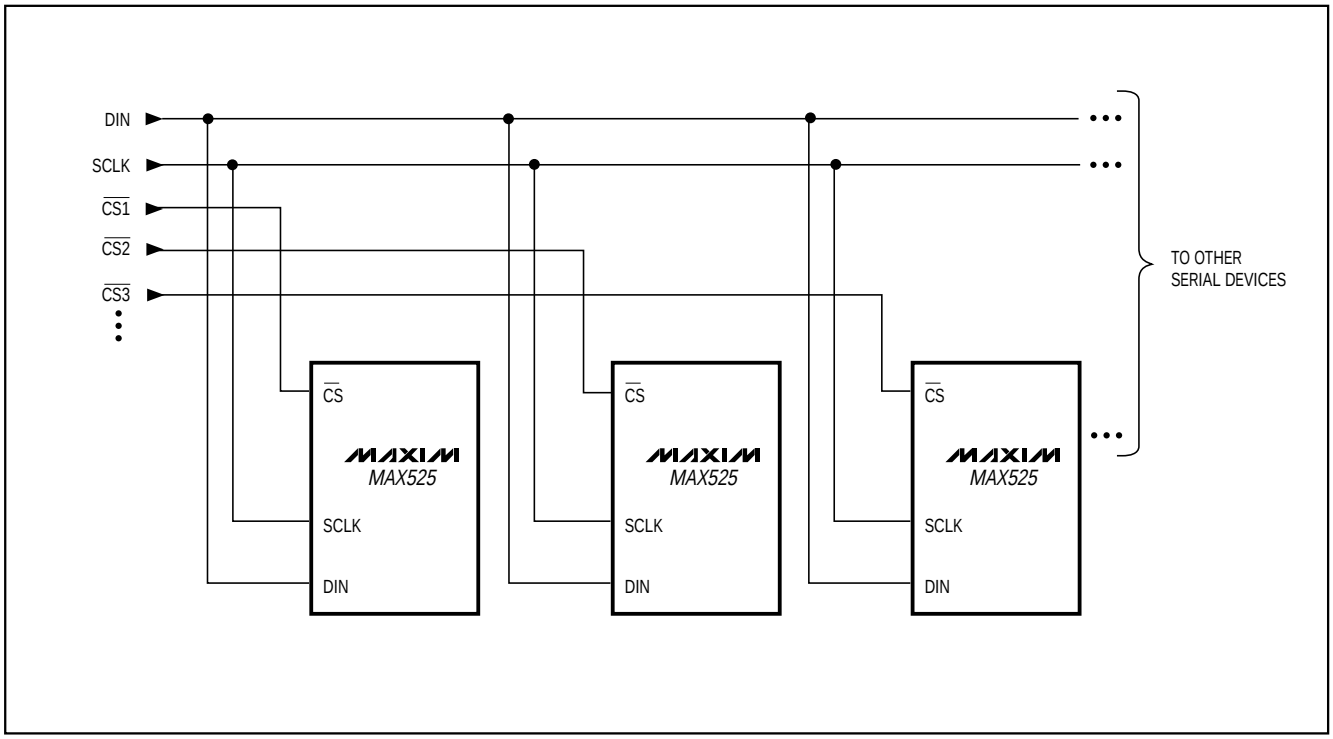


Figure 8. Multiple MAX525s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX525 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX525 with the output amplifiers configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$+V_{REF}\left(\frac{2048}{4096}\right) = \frac{+V_{REF}}{2}$
0111 1111 1111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

Note: 1LSB = $(V_{REF})\left(\frac{1}{4096}\right)$

Bipolar Output

The MAX525 outputs can be configured for bipolar operation using Figure 11's circuit.

$$V_{OUT} = V_{REF}\,[(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

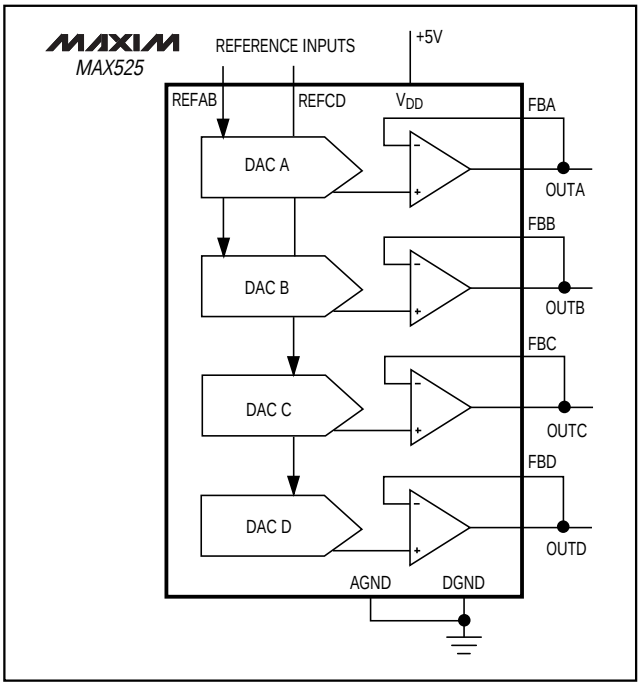


Figure 9. Unipolar Output Circuit

Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

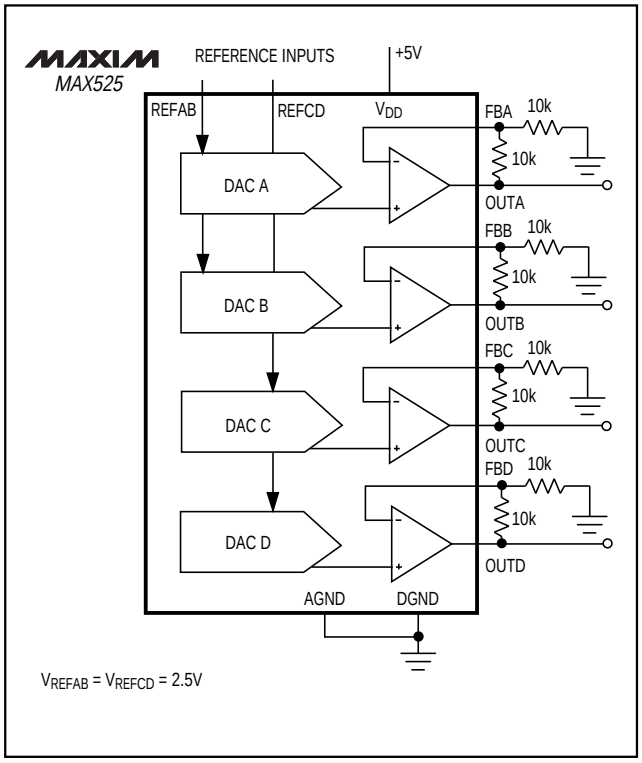


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX525 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX525's total harmonic distortion plus noise (THD + N) is typically less than -72dB, given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4mA to 20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

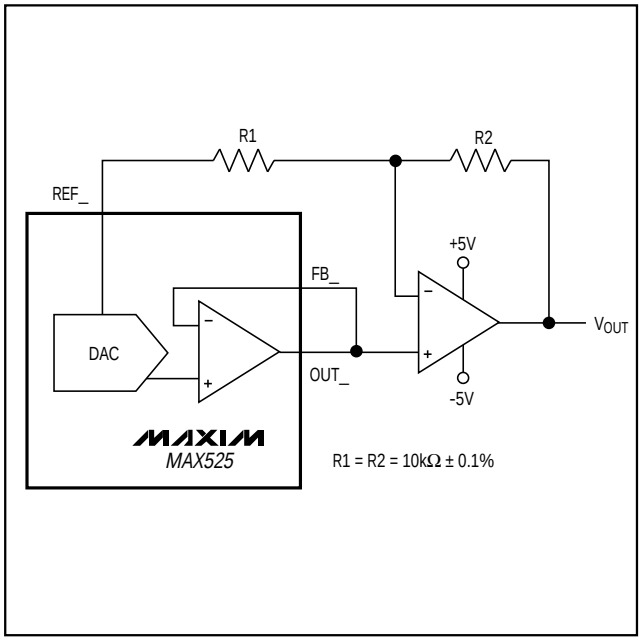


Figure 11. Bipolar Output Circuit

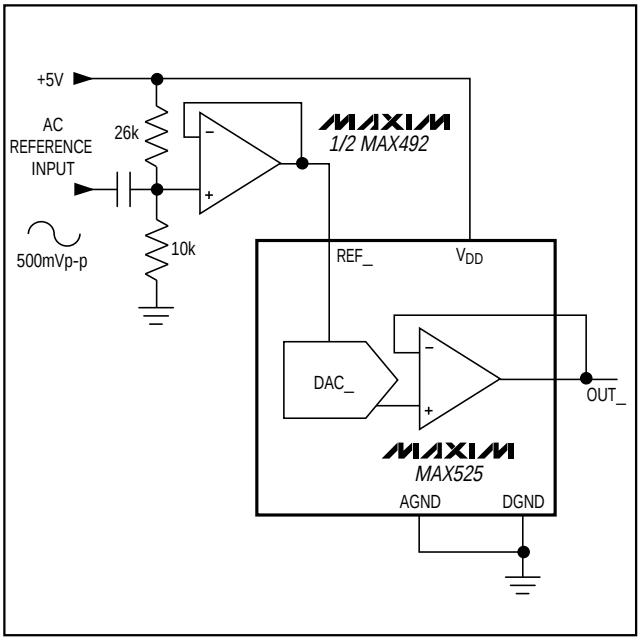


Figure 12. AC Reference Input Circuit

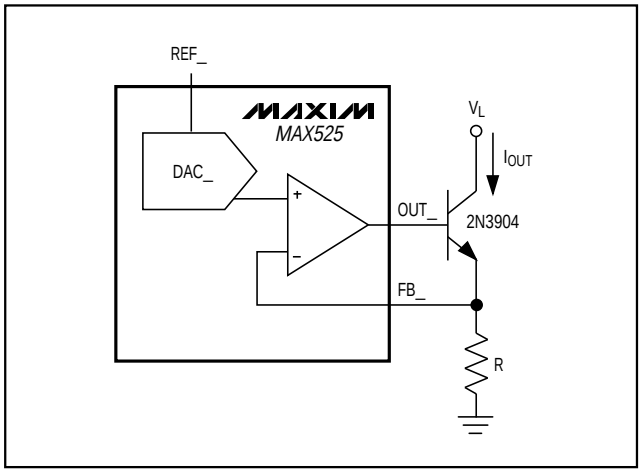


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

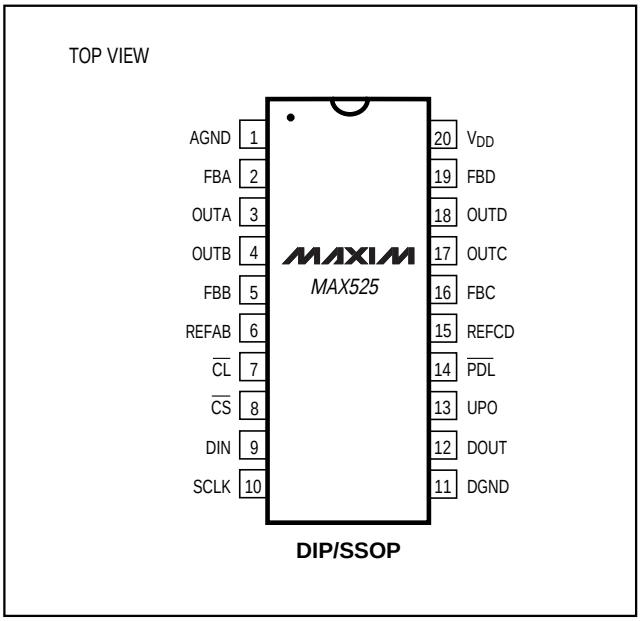
For rated MAX525 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



Low-Power, Quad, 12-Bit Voltage-Output DAC with Serial Interface

Ordering Information (continued)

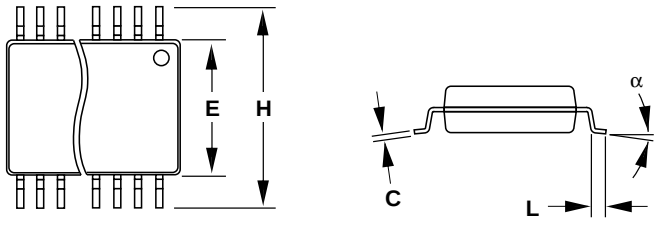
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX525BC/D	0°C to +70°C	Dice*	±1
MAX525AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX525BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX525AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX525BEAP	-40°C to +85°C	20 SSOP	±1
MAX525AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX525BMJP	-55°C to +125°C	20 CERDIP**	±1

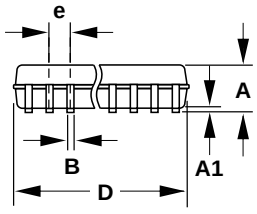
** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 4337

Package Information





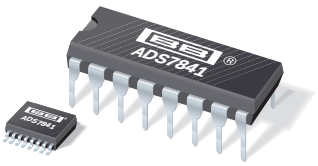
SSOP SHRINK SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	14	0.239	0.249	6.07	6.33
D	16	0.239	0.249	6.07	6.33
D	20	0.278	0.289	7.07	7.33
D	24	0.317	0.328	8.07	8.33
D	28	0.397	0.407	10.07	10.33

21-0056A

ADS7841



SBOS084A – NOVEMBER 2000

12-Bit, 4-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- SINGLE SUPPLY: 2.7V to 5V
- 4-CHANNEL SINGLE-ENDED OR 2-CHANNEL DIFFERENTIAL INPUT
- UP TO 200kHz CONVERSION RATE
- ±1 LSB MAX INL AND DNL
- GUARANTEED NO MISSING CODES
- 72dB SINAD
- SERIAL INTERFACE
- DIP-16 OR SSOP-16 PACKAGE
- ALTERNATE SOURCE FOR MAX1247

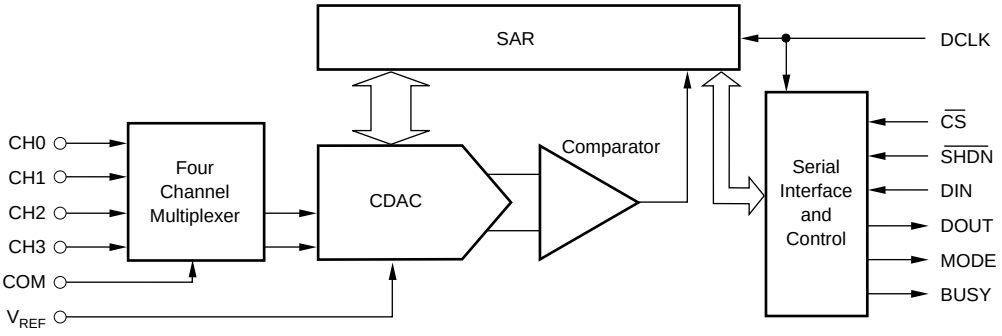
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS7841 is a 4-channel, 12-bit sampling Analog-to-Digital Converter (ADC) with a synchronous serial interface. The resolution is programmable to either 8 bits or 12 bits. Typical power dissipation is 2mW at a 200kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 100mV and V_{CC}, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode which reduces power dissipation to under 15µW. The ADS7841 is guaranteed down to 2.7V operation.

Low power, high speed, and on-board multiplexer make the ADS7841 ideal for battery operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS7841 is available in a DIP-16 or a SSOP-16 package and is guaranteed over the –40°C to +85°C temperature range.



SPECIFICATION: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+1.25	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				200			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 5Vp-p at 10kHz		–78	–72		–80	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz	72	79		76	81		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		120			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	3.0		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			550	900			*	µA
	f_{SAMPLE} = 12.5kHz		300			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				4.5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 1.22mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

SPECIFICATION: +2.7V

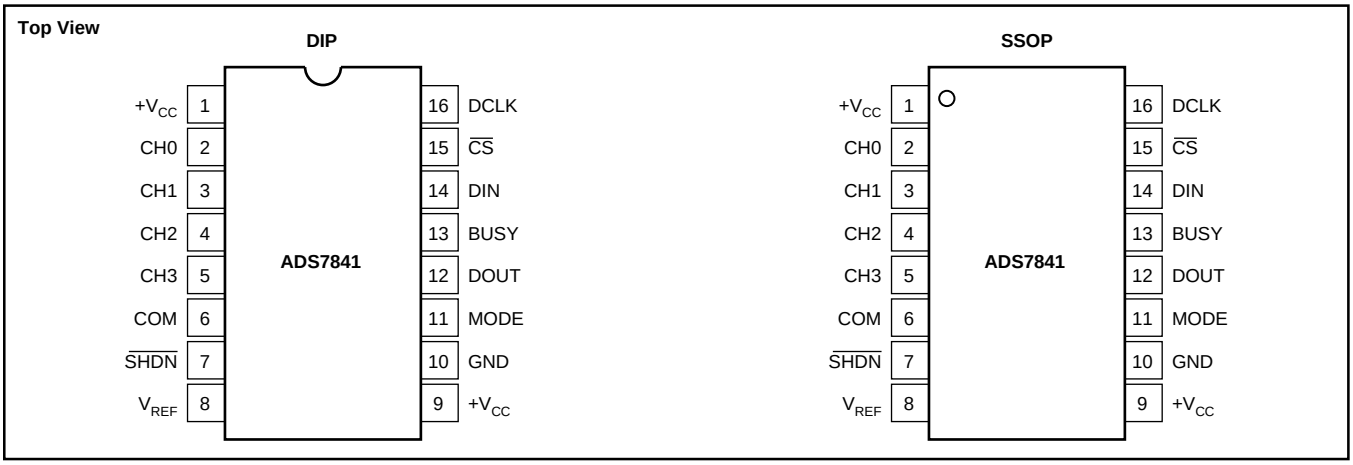
At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS7841E, P			ADS7841EB, PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ +0.2	*		*	V
	Negative Input	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
Resolution			12			*		Bits
No Missing Codes		12			12			Bits
Integral Linearity Error				±2			±1	LSB[1]
Differential Linearity Error			±0.8			±0.5	±1	LSB
Offset Error				±3			*	LSB
Offset Error Match			0.15	1.0		*	*	LSB
Gain Error				±4			±3	LSB
Gain Error Match			0.1	1.0		*	*	LSB
Noise			30			*		µVrms
Power Supply Rejection			70			*		dB
SAMPLING DYNAMICS								
Conversion Time				12			*	Clk Cycles
Acquisition Time		3			*			Clk Cycles
Throughput Rate				125			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 10kHz		–77	–72		–79	–76	dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 10kHz	68	71		70	72		dB
Spurious Free Dynamic Range	V_{IN} = 2.5Vp-p at 10kHz	72	78		76	80		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100			*		dB
REFERENCE INPUT								
Range		0.1		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	$\lvert I_{IH} \rvert \leq +5\mu A$	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	$\lvert I_{IL} \rvert \leq +5\mu A$	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			280	650		*	*	µA
	f_{SAMPLE} = 12.5kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation				1.8			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS7841E, P.

NOTE: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 610mV. (2) First five harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_{CC}$	Power Supply, 2.7V to 5V.
2	CH0	Analog Input Channel 0.
3	CH1	Analog Input Channel 1.
4	CH2	Analog Input Channel 2.
5	CH3	Analog Input Channel 3.
6	COM	Ground Reference for Analog Inputs. Sets zero code voltage in single-ended mode. Connect this pin to ground or ground reference point.
7	$\overline{SHDN}$	Shutdown. When LOW, the device enters a very low power shutdown mode.
8	V_{REF}	Voltage Reference Input
9	$+V_{CC}$	Power Supply, 2.7V to 5V.
10	GND	Ground
11	MODE	Conversion Mode. When LOW, the device always performs a 12-bit conversion. When HIGH, the resolution is set by the MODE bit in the CONTROL byte.
12	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
13	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is HIGH.
14	DIN	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of DCLK.
15	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register.
16	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

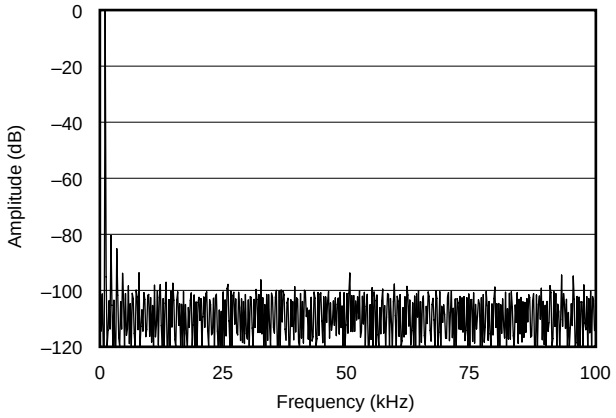
PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS7841E	±2	±4	–40°C to +85°C	16-Lead SSOP	322	ADS7841E	Rails
"	"	"	"	"	"	ADS7841E/2K5	Tape and Reel
ADS7841P	±2	"	–40°C to +85°C	16-Pin PDIP	180	ADS7841P	Rails
ADS7841EB	±1	±3	–40°C to +85°C	16-Lead SSOP	322	ADS7841EB	Rails
"	"	"	"	"	"	ADS7841EB/2K5	Tape and Reel
ADS7841PB	±1	"	–40°C to +85°C	16-Pin PDIP	180	ADS7841PB	Rails

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS7841E/2K5" will get a single 2500-piece Tape and Reel.

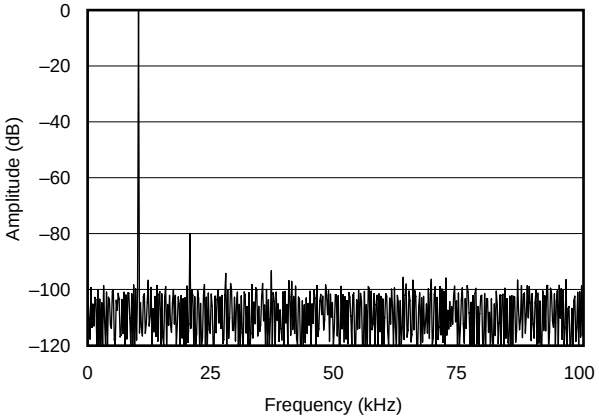
TYPICAL PERFORMANCE CURVES:+5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE} = 3.2MHz, unless otherwise noted.

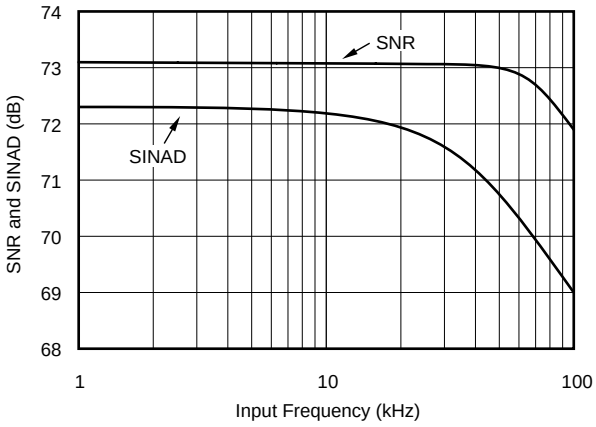
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,123Hz, –0.2dB)



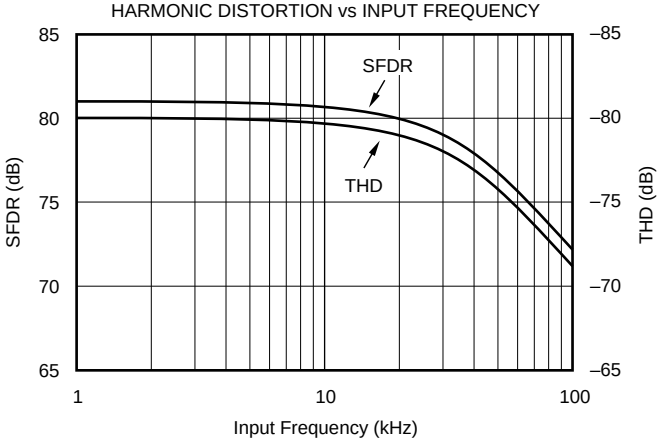
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.3kHz, –0.2dB)



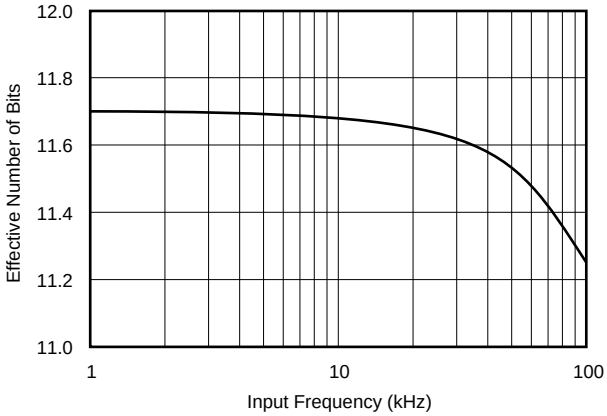
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



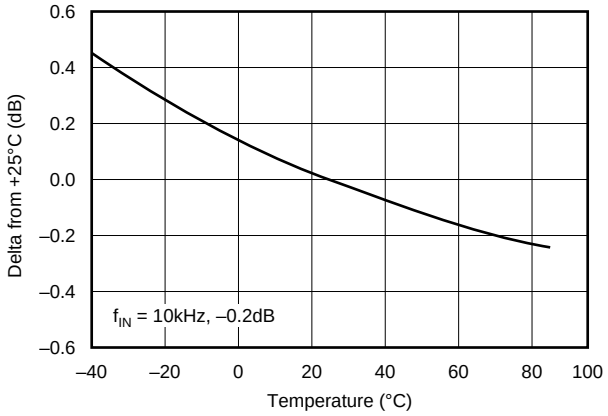
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



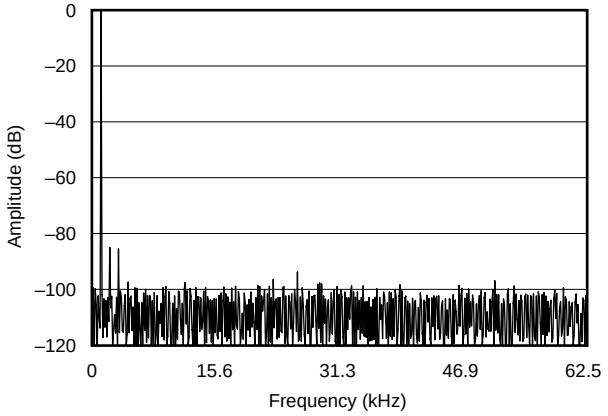
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



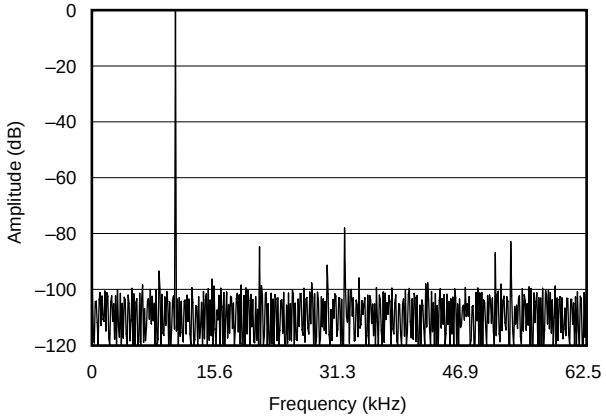
TYPICAL PERFORMANCE CURVES:+2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

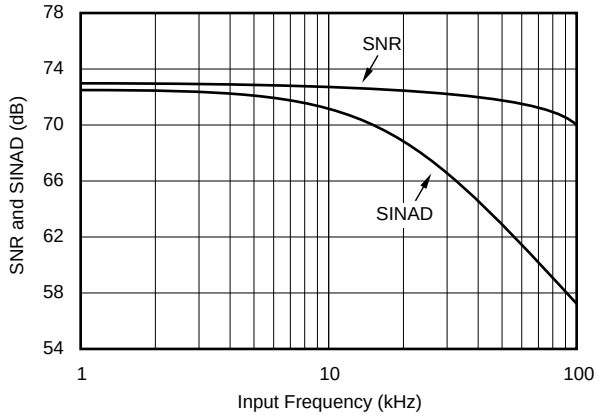
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1,129Hz, –0.2dB)



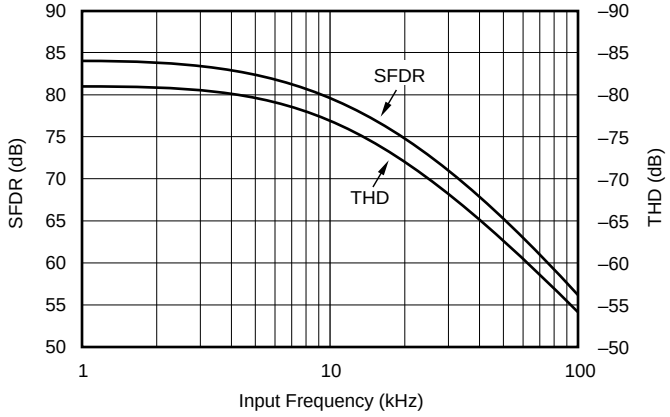
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 10.6kHz, –0.2dB)



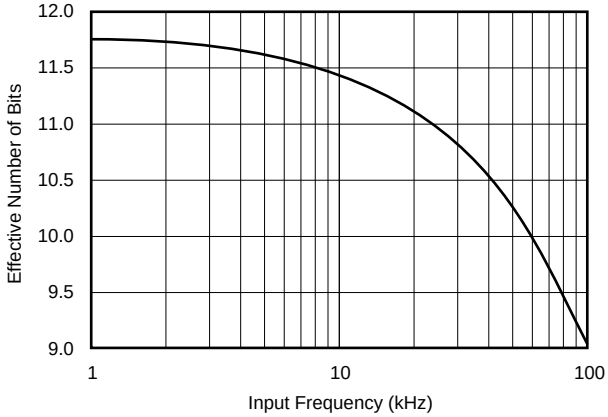
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



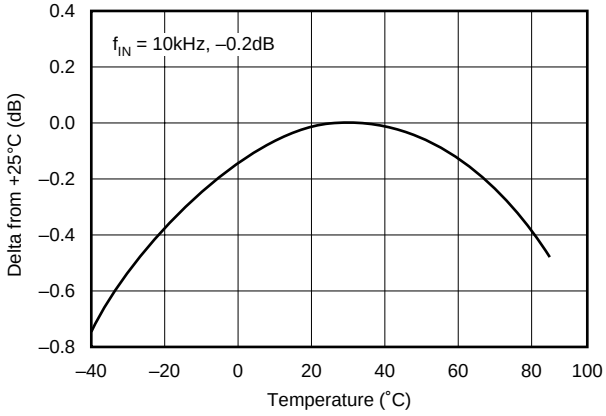
SPURIOUS FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



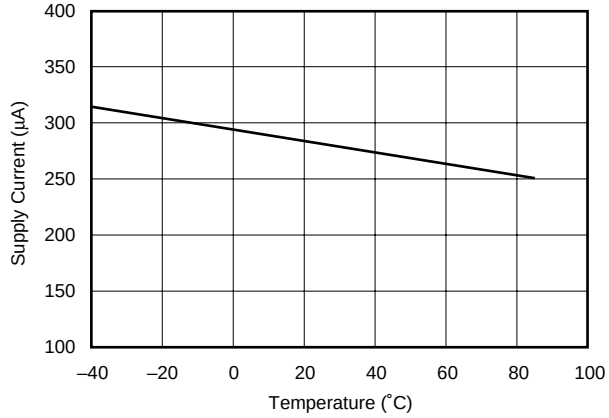
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



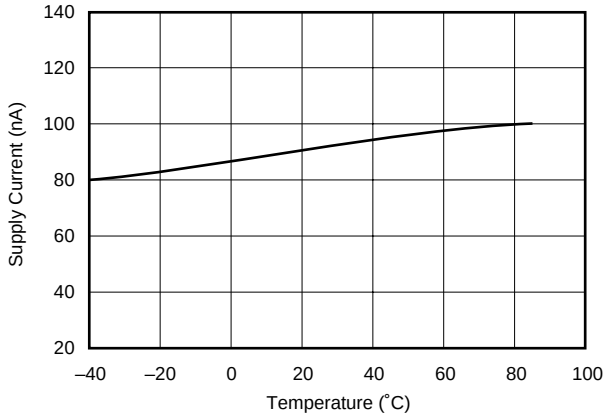
TYPICAL PERFORMANCE CURVES:+2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

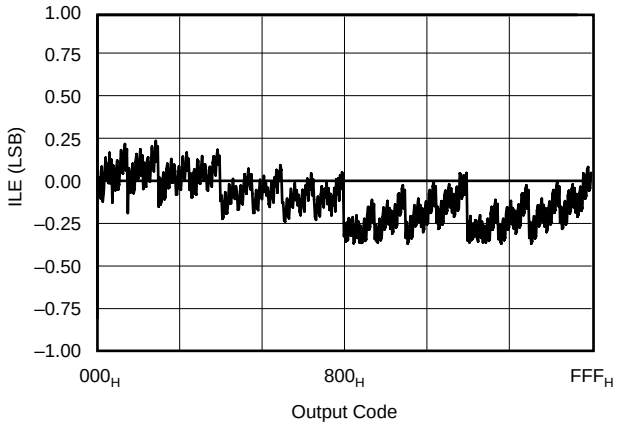
SUPPLY CURRENT vs TEMPERATURE



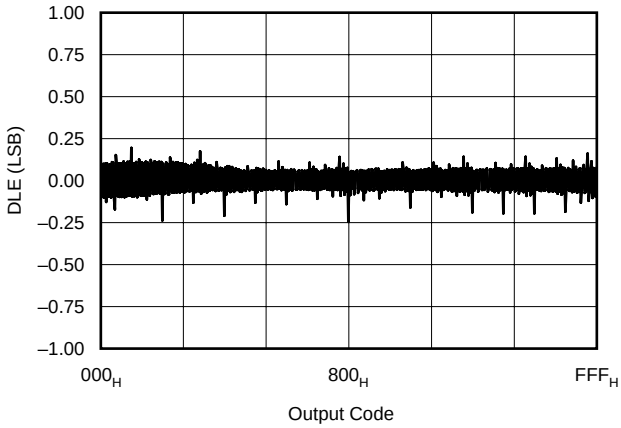
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



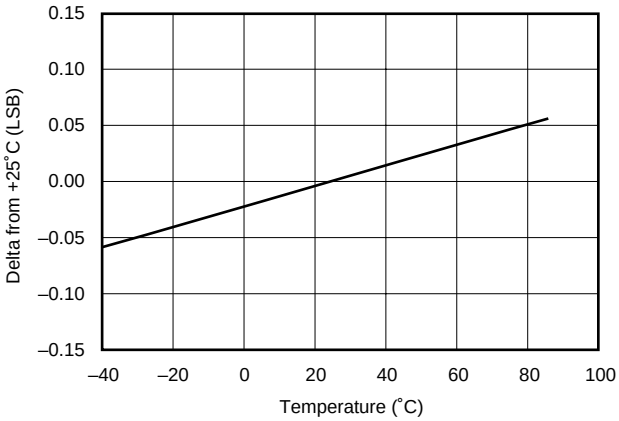
INTEGRAL LINEARITY ERROR vs CODE



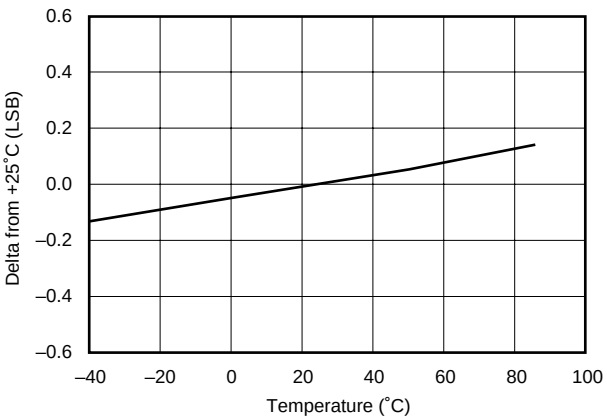
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN GAIN vs TEMPERATURE



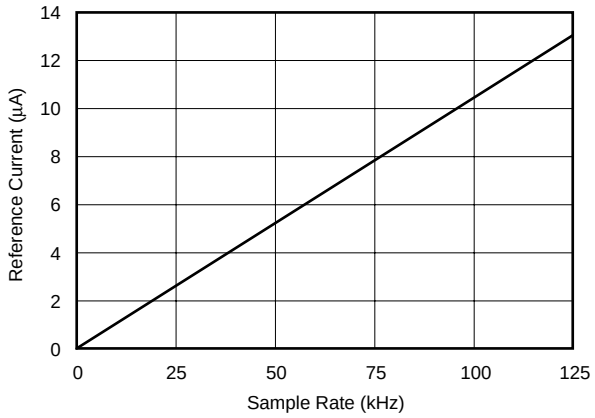
CHANGE IN OFFSET vs TEMPERATURE



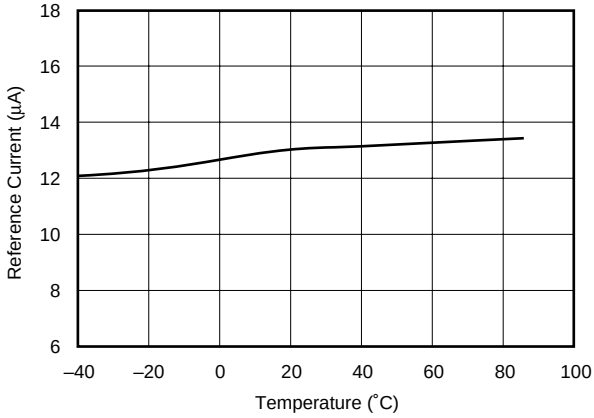
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.5V, f_{SAMPLE} = 125kHz, and f_{CLK} = 16 • f_{SAMPLE} = 2MHz, unless otherwise noted.

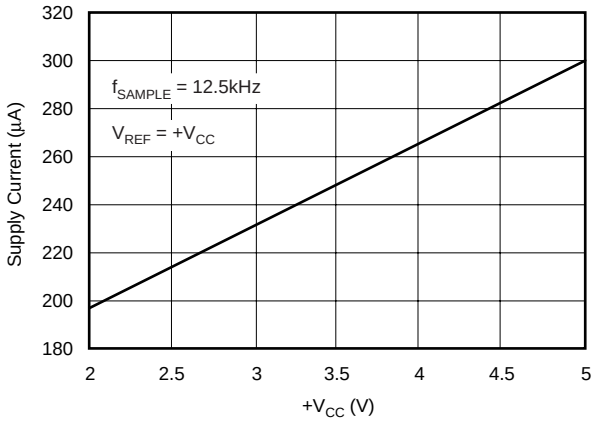
REFERENCE CURRENT vs SAMPLE RATE



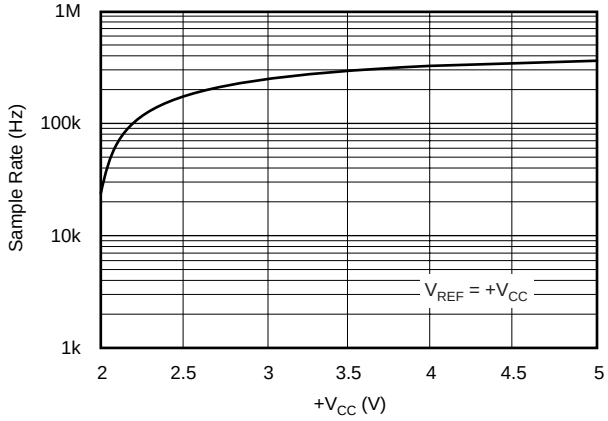
REFERENCE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{CC}$



MAXIMUM SAMPLE RATE vs $+V_{CC}$



THEORY OF OPERATION

The ADS7841 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS7841 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 100mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS7841.

The analog input to the converter is differential and is provided via a four-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using two of the four input channels (CH0 - CH3). The particular configuration is selectable via the digital interface.

ANALOG INPUT

Figure 2 shows a block diagram of the input multiplexer on the ADS7841. The differential input of the converter is derived from one of the four inputs in reference to the COM pin or two of the four inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/$\overline{\text{DIF}}$ control bits and the configuration of the analog multiplexer. The control bits are provided serially via the DIN pin, see the Digital Interface section of this data sheet for more details.

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs (see Figure 2) is captured on the internal capacitor array. The voltage on the –IN input is limited between –0.2V and 1.25V, allowing the input to reject small signals which are common to both the +IN and –IN input. The +IN input has a range of –0.2V to $+V_{CC}$ + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN				–IN
1	0	1		+IN			–IN
0	1	0			+IN		–IN
1	1	0				+IN	–IN

TABLE I. Single-Ended Channel Selection (SGL/$\overline{\text{DIF}}$ HIGH).

A2	A1	A0	CH0	CH1	CH2	CH3	COM
0	0	1	+IN	–IN			
1	0	1	–IN	+IN			
0	1	0			+IN	–IN	
1	1	0			–IN	+IN	

TABLE II. Differential Channel Control (SGL/$\overline{\text{DIF}}$ LOW).

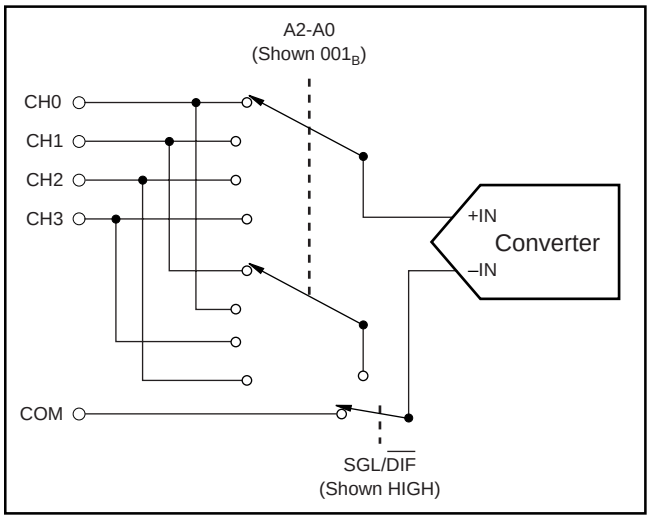


FIGURE 2. Simplified Diagram of the Analog Input.

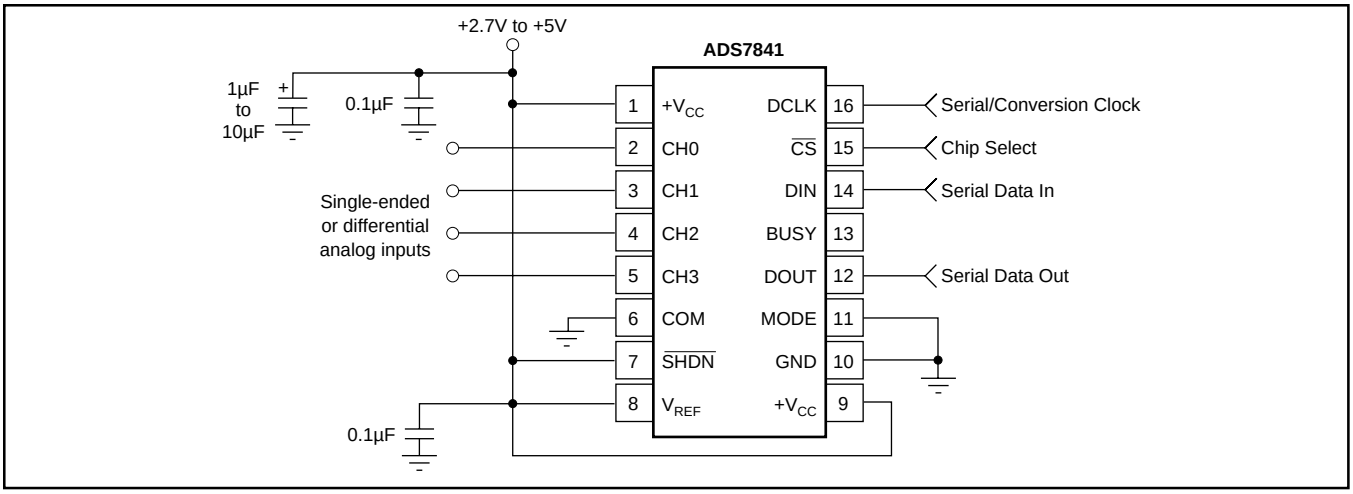


FIGURE 1. Basic Operation of the ADS7841.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7841 will operate with a reference in the range of 100mV to $+V_{CC}$. Keep in mind that the analog input is the difference between the +IN input and the –IN input as shown in Figure 2. For example, in the single-ended mode, a 1.25V reference, and with the COM pin grounded, the selected input channel (CH0 - CH3) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 4096. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2 LSBs with a 2.5V reference, then it will typically be 10 LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 1.22mV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 100mV, the LSB size is 24μV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low noise, low ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the capacitor digital-to-analog converter (CDAC) portion of the ADS7841. Typically, the input current is 13μA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

Figure 3 shows the typical operation of the ADS7841's digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface (note that the digital inputs are over-voltage tolerant up to 5.5V, regardless of $+V_{CC}$). Each communication between the processor and the converter consists of eight clock cycles. One complete conversion can be accomplished with three serial communications, for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample/hold goes into the hold mode. The next twelve clock cycles accomplish the actual analog-to-digital conversion. A thirteenth clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be LOW). These will be ignored by the converter.

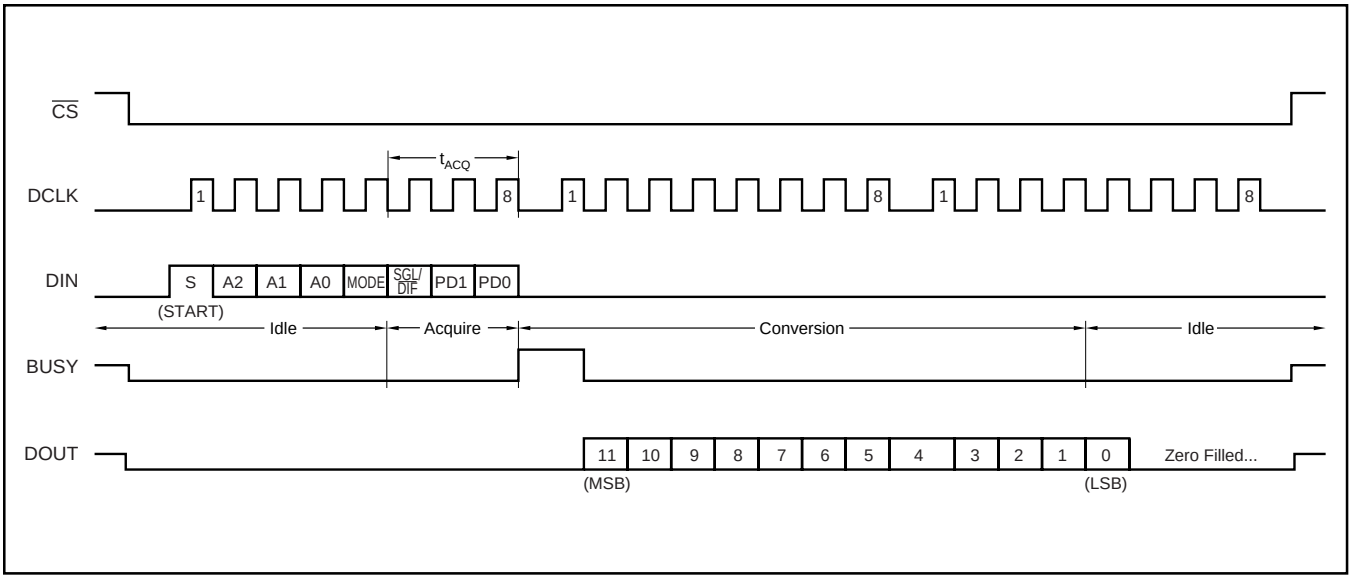


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

Control Byte

Also shown in Figure 3 is the placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the 'S' bit, must always be HIGH and indicates the start of the control byte. The ADS7841 will ignore inputs on the DIN pin until the start bit is detected. The next three bits (A2 - A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on DIN. A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/DIF bit, these bits control the setting of the multiplexer input as detailed in Tables I and II.
3	MODE	12-Bit/8-Bit Conversion Select Bit. If the MODE pin is HIGH, this bit controls the number of bits for the next conversion: 12-bits (LOW) or 8-bits (HIGH). If the MODE pin is LOW, this bit has no function and the conversion is always 12 bits.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input as detailed in Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

The MODE bit and the MODE pin work together to determine the number of bits for a given conversion. If the MODE pin is LOW, the converter always performs a 12-bit conversion regardless of the state of the MODE bit. If the MODE pin is HIGH, then the MODE bit determines the number of bits for each conversion, either 12 bits (LOW) or 8 bits (HIGH).

The SGL/$\overline{\text{DIF}}$ bit controls the multiplexer input mode: either single-ended (HIGH) or differential (LOW). In single-ended mode, the selected input channel is referenced to the COM pin. In differential mode, the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode as shown in Table V. If both inputs are HIGH, the device is always powered up. If both inputs are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

16-Clocks per Conversion

The control bits for conversion n+1 can be overlapped with conversion 'n' to allow for a conversion every 16 clock cycles, as shown in Figure 4. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer between the processor and the converter. This is possible provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that has been captured on the input sample/hold may droop enough to affect the conversion result. In addition, the ADS7841 is fully powered while other serial communications are taking place.

PD1	PD0	Description
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
0	1	Reserved for future use.
1	0	Reserved for future use.
1	1	No power-down between conversions, device always powered.

TABLE V. Power-Down Selection.

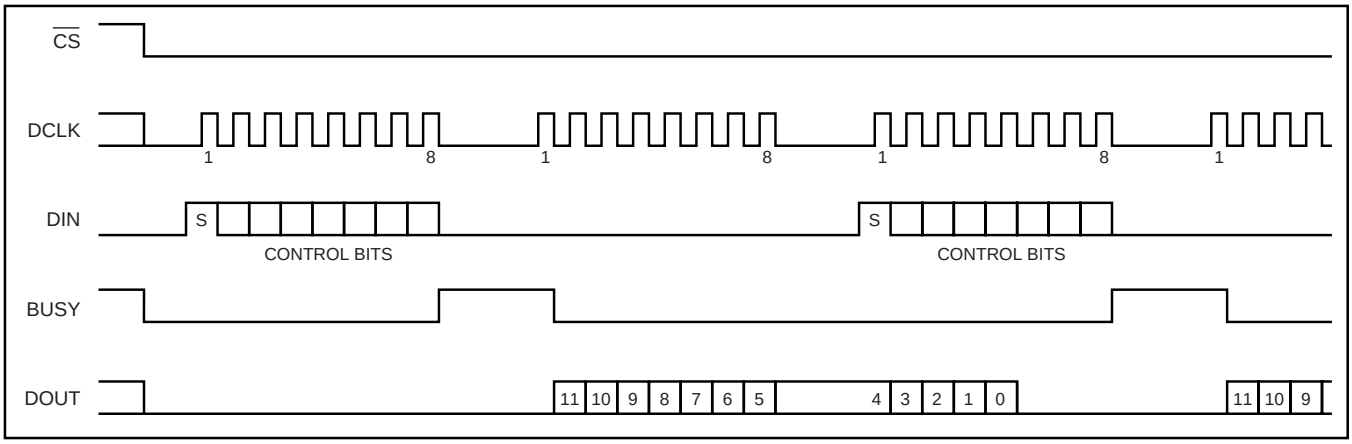


FIGURE 4. Conversion Timing, 16-Clocks per Conversion, 8-bit Bus Interface. No DCLK delay required with dedicated serial port.

Digital Timing

Figure 5 and Tables VI and VII provide detailed timing for the digital interface of the ADS7841.

15-Clocks per Conversion

Figure 6 provides the fastest way to clock the ADS7841. This method will not work with the serial interface of most microcontrollers and digital signal processors as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method could be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	900			ns
t_{DS}	DIN Valid Prior to DCLK Rising	50			ns
t_{DH}	DIN Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to DOUT Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

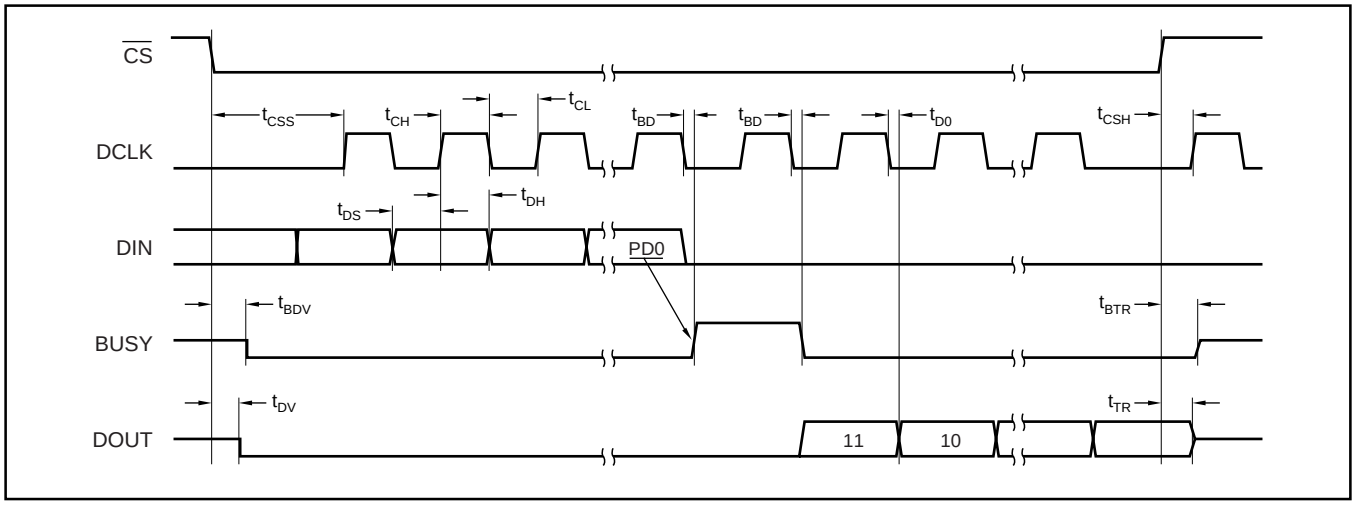


FIGURE 5. Detailed Timing Diagram.

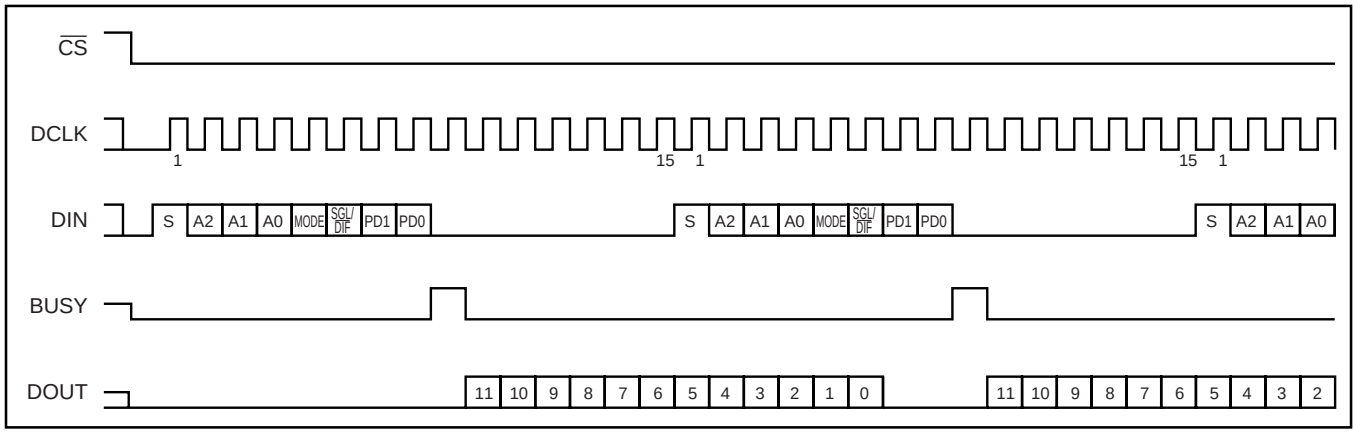


FIGURE 6. Maximum Conversion Rate, 15-Clocks per Conversion.

Data Format

The ADS7841 output data is in straight binary format as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

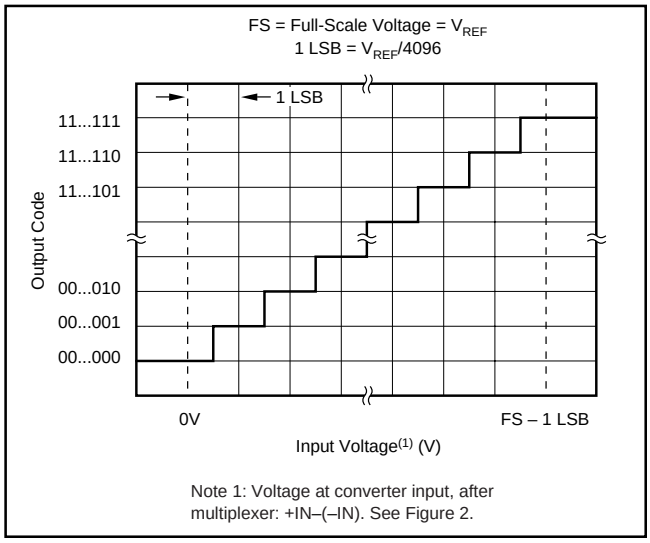


FIGURE 7. Ideal Input Voltages and Output Codes.

8-Bit Conversion

The ADS7841 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. This could be used in conjunction with serial interfaces that provide a 12-bit transfer or two conversions could be accomplished with three 8-bit transfers. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the ADS7841 is not as critical, settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

POWER DISSIPATION

There are three power modes for the ADS7841: full power (PD1 - PD0 = 11B), auto power-down (PD1 - PD0 = 00B), and shutdown ($\overline{SHDN}$ LOW). The affects of these modes varies depending on how the ADS7841 is being operated. For example, at full conversion rate and 16 clocks per conversion, there is very little difference between full power mode and auto power-down. Likewise, if the device has entered auto power-down, a shutdown ($\overline{SHDN}$ LOW) will not lower power dissipation.

When operating at full-speed and 16-clocks per conversion (as shown in Figure 4), the ADS7841 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversion are simply done less often, then the difference between the two modes is dramatic. Figure 8 shows the difference between reducing the DCLK frequency ("scaling" DCLK to match the conversion rate) or maintaining DCLK at the highest frequency and reducing the number of conversion per second. In the later case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and $\overline{CS}$ is LOW while the ADS7841 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ HIGH. The differences in supply current for these two cases are shown in Figure 9.

Operating the ADS7841 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. $\overline{SHDN}$ can be used to force an immediate power-down.

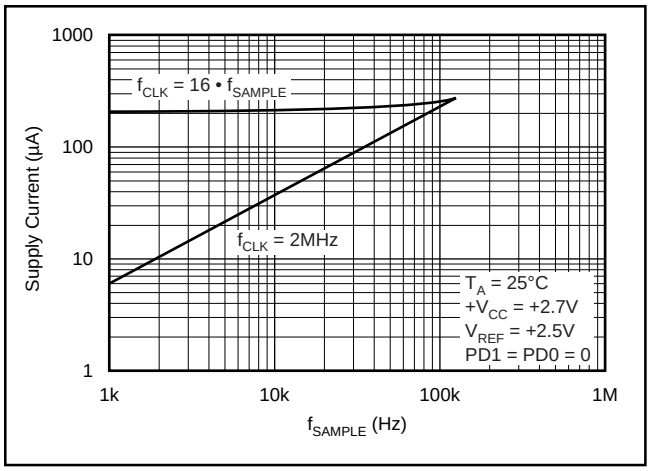


FIGURE 8. Supply Current vs Directly Scaling the Frequency of DCLK with Sample Rate or Keeping DCLK at the Maximum Possible Frequency.

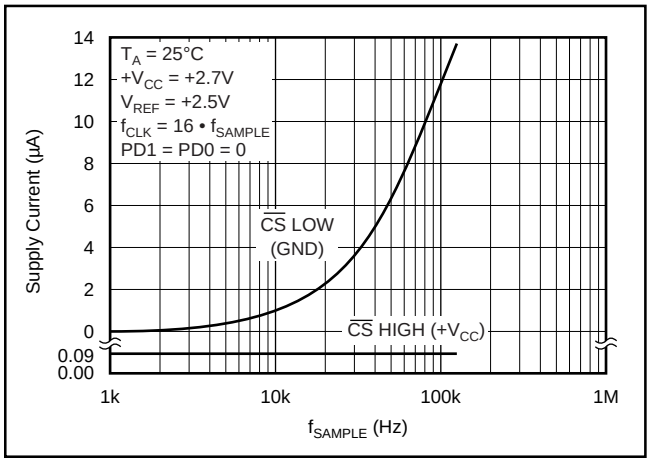


FIGURE 9. Supply Current vs State of $\overline{CS}$.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7841 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS7841 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS7841 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS7841 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with *statements different from or beyond the parameters* stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

National Semiconductor

January 2001

LM4051
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4051 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SSOT-23 surface-mount package. The LM4051's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4051 easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60 µA for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12 mA.

The LM4051 comes in three grades (A, B, and C). The best grade devices (A) have an initial accuracy of 0.1%, while the B-grade have 0.2% and the C-grade 0.5%, all with a tempco of 50 ppm/˚C guaranteed from −40˚C to 125˚C.

The LM4051 utilizes fuse and zener-zap trim of reference voltage during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25˚C.

Features

- Small packages: SSOT-23
- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable

Key Specifications (LM4051-1.2)

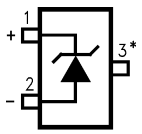
- Output voltage tolerance (A grade, 25˚C) ±0.1%(max)
- Low output noise (10 Hz to 10kHz) $20\mu V_{rms}$
- Wide operating current range 60µA to 12mA
- Industrial temperature range (tempco guaranteed from −40˚C to +125˚C) −40˚C to +85˚C
- Low temperature coefficient 50 ppm/˚C (max)

Applications

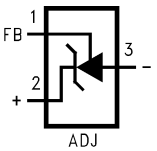
- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Automotive and Industrial
- Precision Audio Components
- Base Stations
- Battery Chargers
- Medical Equipment
- Communication

Connection Diagrams

SSOT-23



DS101222-1



DS101222-40

*This pin must be left floating or connected to pin 2.

Top View
See NS Package Number MF03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25˚C and Average Reverse Breakdown Voltage Temperature Coefficient	LM4051 Supplied as 1000 Units, Tape and Reel	LM4051 Supplied as 3000 Units, Tape and Reel	Part Marking
±0.1%, 50 ppm/˚C max (A grade)	LM4051AIM3-1.2	LM4051AIM3X-1.2	RHA
	LM4051AIM3-ADJ	LM4051AIM3X-ADJ	RIA
±0.2%, 50 ppm/˚C max (B grade)	LM4051BIM3-1.2	LM4051BIM3X-1.2	RHB
	LM4051BIM3-ADJ	LM4051BIM3X-ADJ	RIB
±0.5%, 50 ppm/˚C max (C grade)	LM4051CIM3-1.2	LM4051CIM3X-1.2	RHC
	LM4051CIM3-ADJ	LM4051CIM3X-ADJ	RIC

SOT-23 Package Marking Information

Only three fields of marking are possible on the SSOT-23's small surface. This table gives the meaning of the three fields.

Field Definition
First Field:
R = Reference
Second Field:
H = 1.225V Voltage Option
I = Adjustable
Third Field:
A–C = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance
A = ±0.1%, B = ±0.2%, C = ±0.5%

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Reverse Current	20 mA
Forward Current	10 mA
Maximum Output Voltage (LM4051-ADJ)	15V
Power Dissipation (T_A = 25˚C) (Note 2)	
M3 Package	280 mW
Storage Temperature	−65˚C to +150˚C
Lead Temperature	
M3 Packages	
Vapor phase (60 seconds)	+215˚C
Infrared (15 seconds)	+220˚C
ESD Susceptibility	
Human Body Model (Note 3)	2 kV
Machine Model (Note 3)	200V

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Operating Ratings (Notes 1, 2)

Temperature Range	($T_{min} \le T_A \le T_{max}$)
Industrial Temperature Range	−40˚C ≤ T_A ≤ +85˚C
Reverse Current	
LM4051-1.2	60 µA to 12 mA
LM4051-ADJ	60 µA to 12 mA
Output Voltage Range	
LM4051-ADJ	1.24V to 10V

LM4051-1.2 Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J$ = 25˚C. The grades A, B and C designate initial Reverse Breakdown Voltage tolerances of ±0.1%, ±0.2% and ±0.5% respectively.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4051AIM3 (Limits) (Note 5)	LM4051BIM3 (Limits) (Note 5)	LM4051CIM3 Limts (Note 5)	Units (Limit)
V_R	Reverse Breakdown Voltage	I_R = 100 µA	1.225				V
	Reverse Breakdown Voltage	I_R = 100 µA		±1.2	±2.4	±6	mV (max)
	Tolerance (Note 6)			**±5.2**	**±6.4**	**±10.1**	mV (max)
I_{RMIN}	Minimum Operating Current		39				µA
				60	60	60	µA (max)
				65	**65**	**65**	µA (max)
$\Delta V_R/\Delta T$	Average Reverse Breakdown Voltage Temperature Coefficient (Note 6)	I_R= 10 mA	±20				ppm/˚C
		I_R = 1 mA	±15				ppm/˚C
		I_R = 100 µA ΔT = −40˚C to 125˚C	±15	**±50**	**±50**	**±50**	ppm/˚C (max)
$\Delta V_R/\Delta I_R$	Reverse Breakdown Voltage Change with Operating Current Change	$I_{RMIN} \le I_R \le$ 1 mA	0.3				mV
				1.1	1.1	1.1	mV (max)
				1.5	**1.5**	**1.5**	mV (max)
		1 mA ≤ I_R ≤ 12 mA	1.8				mV
				6.0	6.0	6.0	mV (max)
				8.0	**8.0**	**8.0**	mV (max)
Z_R	Reverse Dynamic Impedance	I_R = 1 mA, f = 120 Hz	0.5				Ω
e_N	Wideband Noise	I_R = 100 µA 10 Hz ≤ f ≤ 10 kHz	20				μV_{rms}
ΔV_R	Reverse Breakdown Voltage Long Term Stability (Note 9)	t = 1000 hrs T = 25˚C ±0.1˚C I_R = 100 µA	120				ppm
V_{HYST}	Output Hysteresis (Note 10)	ΔT = −40˚C to 125˚C	0.36				mV/V

LM4051-ADJ (Adjustable) Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits T_J = 25˚C unless otherwise specified (SSOT-23, see (Note 7) , $I_{RMIN} \le I_R \le 12$ mA, $V_{REF} \le V_{OUT} \le 10$V. The grades A, B and C designate initial Reference Voltage Tolerances of ±0.1%, ±0.2% and ±0.5%, respectively for V_{OUT} = 5V.

Symbol	Parameter	Conditions	Typical (Note 4)	LM4051AIM3 (Note 5)	LM4051BIM3 (Note 5)	LM4051CIM3 (Note 5)	Units (Limit)
V_{REF}	Reference Voltage	I_R = 100 µA, V_{OUT} = 5V	1.212				V
	Reference Voltage Tolerance (Note 6), (Note 8)	I_R = 100 µA, V_{OUT} = 5V		±1.2 **±5.2**	±2.4 **±6.4**	±6 **±10.1**	mV (max) mV (max)
I_{RMIN}	Minimum Operating Current		36	 60 **65**	 60 **65**	 65 **70**	µA µA (max) µA (max)
$\Delta V_{REF}/\Delta I_R$	Reference VoltageChange with Operating Current Change	$I_{RMIN} \le I_R \le$ 1mA $V_{OUT} \ge$ 1.6V (Note 7)	0.3	 1.1 **1.5**	 1.1 **1.5**	 1.1 **1.5**	mV mV (max) mV(max)
		1 mA $\le I_R \le$ 12 mA $V_{OUT} \ge$ 1.6V(Note 7)	0.6	 6 **8**	 6 **8**	 6 **8**	mV mV (max) mV (max)
$\Delta V_{REF}/\Delta V_O$	Reference Voltage Changewith Output Voltage Change	I_R = 0.1 mA	−1.69	 −2.8 **−3.5**	 −2.8 **−3.5**	 −2.8 **−3.5**	mV/V mV/V (max) mV/V (max)
I_{FB}	Feedback Current		70	 130 **150**	 130 **150**	 130 **150**	nA nA (max) nA (max)
$\Delta V_{REF}/\Delta T$	Average ReferenceVoltage Temperature Coefficient (Note 8)	V_{OUT} = 2.5V I_R = 10mA I_R = 1mA I_R = 100µA ΔT = −40˚C to +125˚C	 20 15 15	 **±50**	 **±50**	 **±50**	 ppm/˚C ppm/˚C ppm/˚C (max)
Z_{OUT}	Dynamic Output Impedance	I_R = 1 mA, f = 120 Hz, $I_{AC} = 0.1\ I_R$ $V_{OUT} = V_{REF}$ V_{OUT} = 10V	 0.3 2				 Ω Ω
e_N	Wideband Noise	I_R = 100 µA $V_{OUT} = V_{REF}$ 10 Hz ≤ f ≤ 10 kHz	20				μV_{rms}
ΔV_{REF}	Reference Voltage Long Term Stability (Note 9)	t = 1000 hrs, I_R = 100 µA T = 25˚C ±0.1˚C	120				ppm
V_{HYST}	Output Hysteresis (Note 10)	ΔT = −40˚C to +125˚C	0.3				mV/V

Electrical Characteristics (continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $PD_{max} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM4051, $T_{Jmax} = 125^{\circ}C$, and the typical thermal resistance (θ_{JA}), when board mounted, is 280˚C/W for the SSOT-23 package.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Typicals are at $T_J = 25^{\circ}C$ and represent most likely parametric norm.

Note 5: Limits are 100% production tested at 25˚C. Limits over temperature are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate National's AOQL.

Note 6: The boldface (over-temperature) limit for Reverse Breakdown Voltage Tolerance is defined as the room temperature Reverse Breakdown Voltage Tolerance $\pm[(\Delta V_R/\Delta T)(\max \Delta T)(V_R)]$. Where, $\Delta V_R/\Delta T$ is the V_R temperature coefficient, $\max\Delta T$ is the maximum difference in temperature from the reference point of 25 ˚C to T_{MAX} or T_{MIN}, and V_R is the reverse breakdown voltage. The total over-temperature tolerance for the different grades in the industrial temperature range where $\max\Delta T = 65^{\circ}C$ is shown below:

A-grade: ±0.425% = ±0.1% ±50 ppm/˚C x 65˚C
B-grade: ±0.522% = ±0.2% ±50 ppm/˚C x 65˚C
C-grade: ±0.825% = ±0.5% ±50 ppm/˚C x 65˚C

Therefore, as an example, the A-grade LM4051-1.2 has an over-temperature Reverse Breakdown Voltage tolerance of ±1.2V x 0.425% = ±5.2 mV.

Note 7: When $V_{OUT} \leq 1.6V$, the LM4051-ADJ in the SSOT-23 package must operate at reduced I_R. This is caused by the series resistance of the die attach between the die (-) output and the package (-) output pin. See the Output Saturation curve in the Typical Performance Characteristics section.

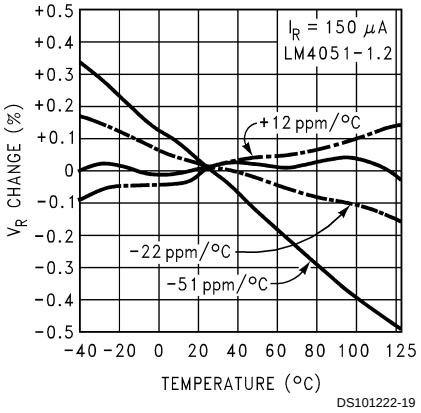
Note 8: Reference voltage and temperature coefficient will change with output voltage. See Typical Performance Characteristics curves.

Note 9: Long term stability is V_R @ 25˚C measured during 1000 hrs.

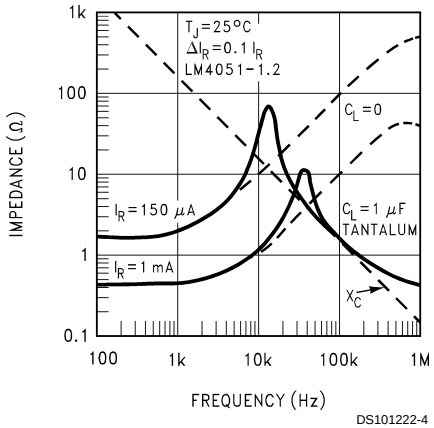
Note 10: Thermal hysteresis is defined as the changes in 25˚C output voltage before and after cycling the device from −40˚C or +125˚C.

Typical Performance Characteristics

Temperature Drift for Different Average Temperature Coefficient

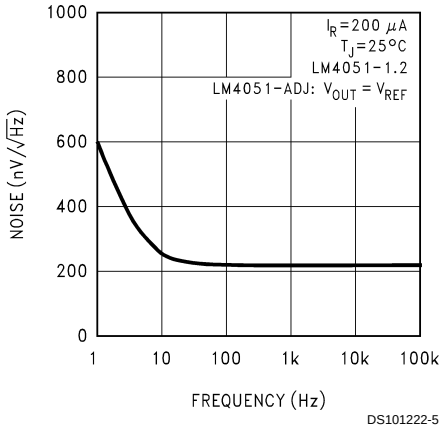


Output Impedance vs Frequency



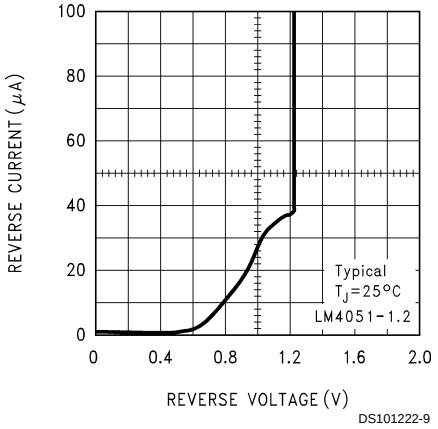
Typical Performance Characteristics (Continued)

Noise Voltage



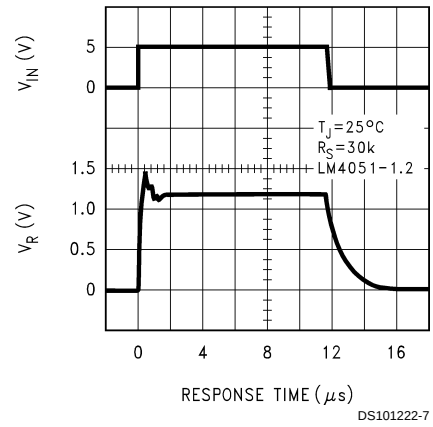
DS101222-5

Reverse Characteristics and Minimum Operating Current

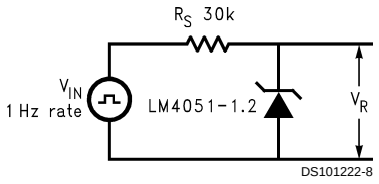


DS101222-9

Start-Up Characteristics

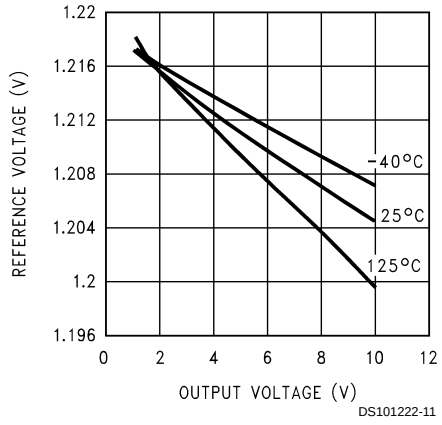


DS101222-7



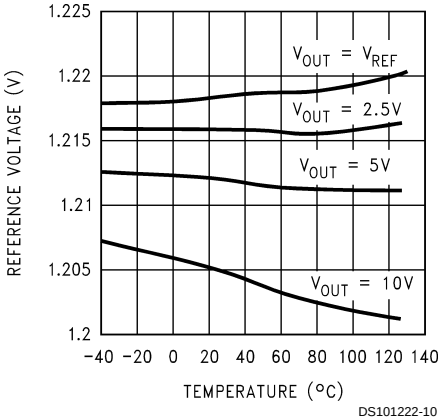
DS101222-8

Reference Voltage vs Output Voltage and Temperature



DS101222-11

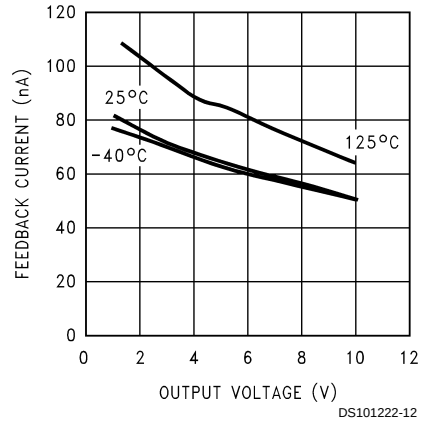
Reference Voltage vs Temperature and Output Voltage



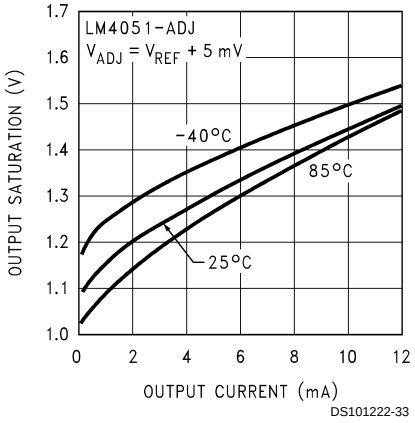
DS101222-10

Typical Performance Characteristics (Continued)

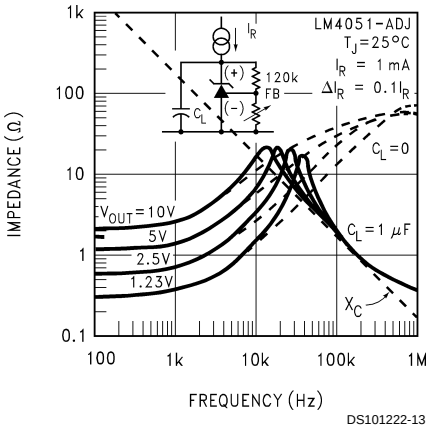
Feedback Current vs Output Voltage and Temperature



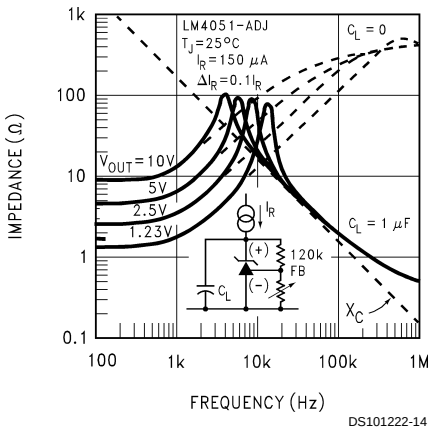
Output Saturation (SOT-23 Only)



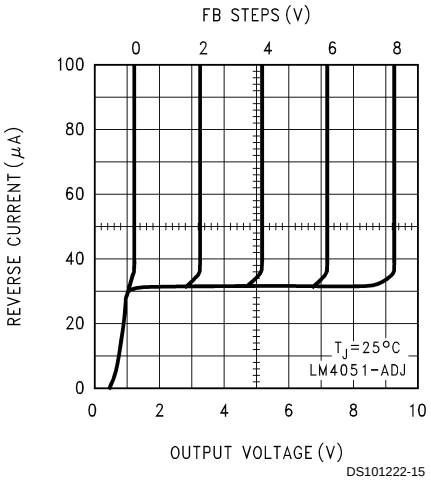
Output Impedance vs Frequency

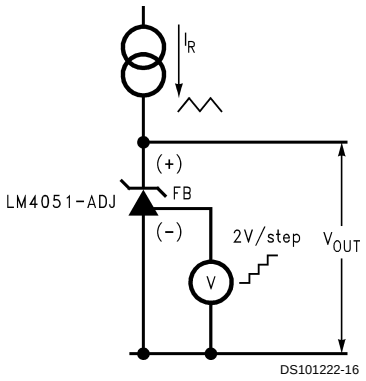


Output Impedance vs Frequency



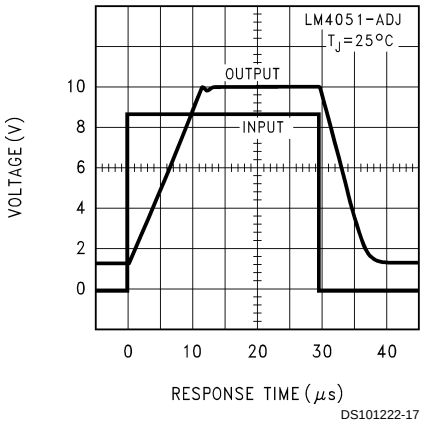
Reverse Characteristics



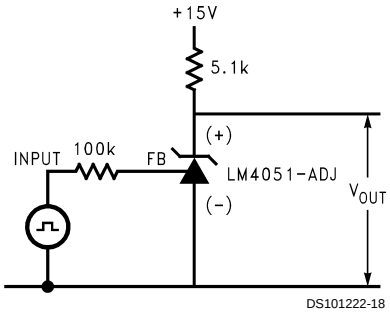


Typical Performance Characteristics (Continued)

Large Signal Response

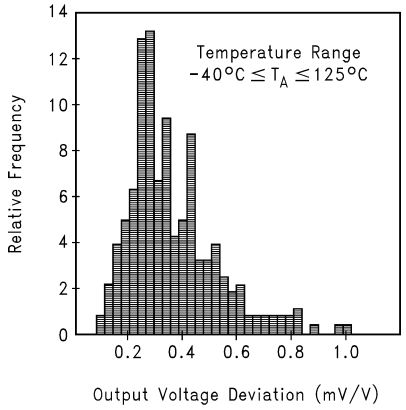


DS101222-17



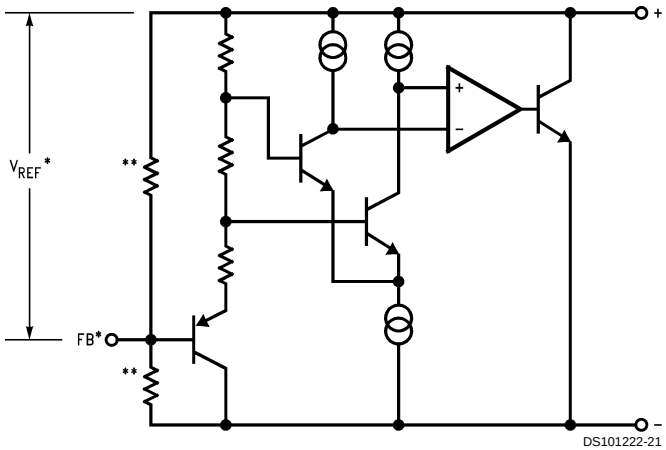
DS101222-18

Thermal Hysteresis



DS101222-50

Functional Block Diagram



DS101222-21

*LM4051-ADJ only
**LM4051-1.2 only

Applications Information

The LM4051 is a precision micro-power curvature-corrected bandgap shunt voltage reference. For space critical applications, the LM4051 is available in the sub-miniature SSOT-23 surface-mount package. The LM4051 has been designed for stable operation without the need of an external capacitor connected between the "+" pin and the "−" pin. If, however, a bypass capacitor is used, the LM4051 remains stable. Design effort is further reduced with the choice of either a fixed 1.2V or an adjustable reverse breakdown voltage. The minimum operating current is 60 µA for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12 mA.

LM4051s using the SSOT-23 package have pin 3 connected as the (-) output through the package's die attach interface. Therefore, the LM4051-1.2's pin 3 must be left floating or connected to pin 2 and the LM4051-ADJ's pin 3 is the (-) output.

In a conventional shunt regulator application *(Figure 1)*, an external series resistor (R_S) is connected between the supply voltage and the LM4051. R_S determines the current that flows through the load (I_L) and the LM4051 (I_Q). Since load current and supply voltage may vary, R_S should be small enough to supply at least the minimum acceptable I_Q to the LM4051 even when the supply voltage is at its minimum and the load current is at its maximum value. When the supply voltage is at its maximum and I_L is at its minimum, R_S should be large enough so that the current flowing through the LM4051 is less than 12 mA.

R_S should be selected based on the supply voltage, (V_S), the desired load and operating current, (I_L and I_Q), and the LM4051's reverse breakdown voltage, V_R.

$$R_S = \frac{V_S - V_R}{I_L + I_Q}$$

The LM4051-ADJ's output voltage can be adjusted to any value in the range of 1.24V through 10V. It is a function of the internal reference voltage (V_{REF}) and the ratio of the external feedback resistors as shown in *Figure 2* . The output voltage is found using the equation

$$V_O = V_{REF}[(R2/R1) + 1] \quad (1)$$

$$R_S = \frac{V_S - V_R}{I_L + I_Q + I_F} \quad (2)$$

where V_O is the output voltage. The actual value of the internal V_{REF} is a function of V_O. The "corrected" V_{REF} is determined by

$$V_{REF} = V_O\,(\Delta V_{REF}/\Delta V_O) + V_Y \quad (3)$$

where

$$V_Y = 1.22V$$

$\Delta V_{REF}/\Delta V_O$ is found in the Electrical Characteristics and is typically −1.55 mV/V. You can get a more accurate indication of the output voltage by replacing the value of V_{REF} in equation (1) with the value found using equation (3).

Typical Applications

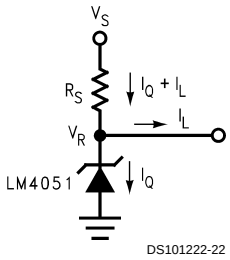


FIGURE 1. Shunt Regulator

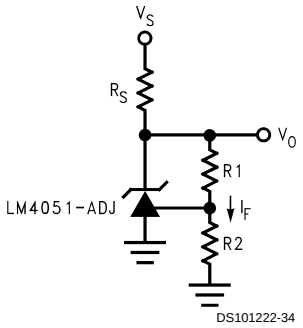


FIGURE 2. Adjustable Shunt Regulator

Typical Applications (Continued)

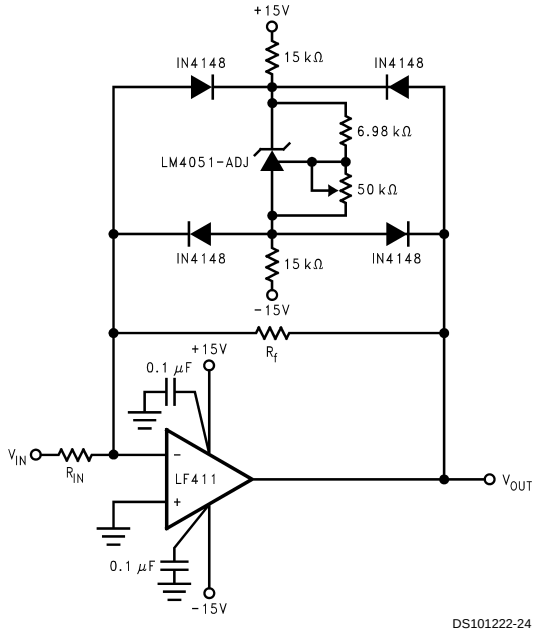


FIGURE 3. Bounded amplifier reduces saturation-induced delays and can prevent succeeding stage damage. Nominal clamping voltage is $\pm V_O$ (LM4051's reverse breakdown voltage) +2 diode V_F.

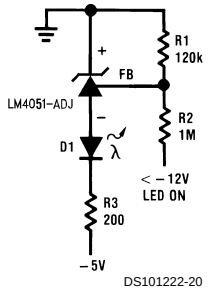


FIGURE 4. Voltage Level Detector

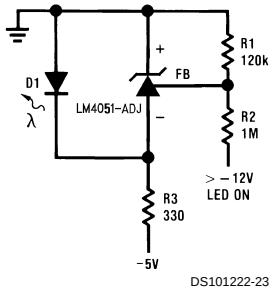


FIGURE 5. Voltage Level Detector

Typical Applications (Continued)

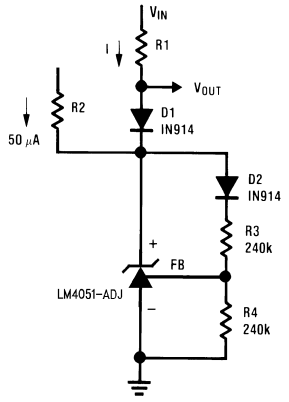


FIGURE 6. Fast Positive Clamp 2.4V + V_{D1}

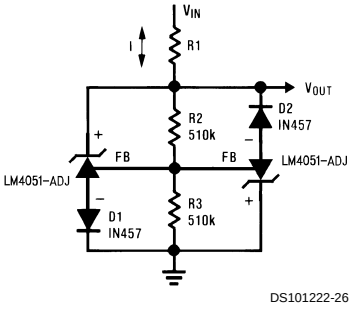


FIGURE 7. Bidirectional Clamp ±2.4V

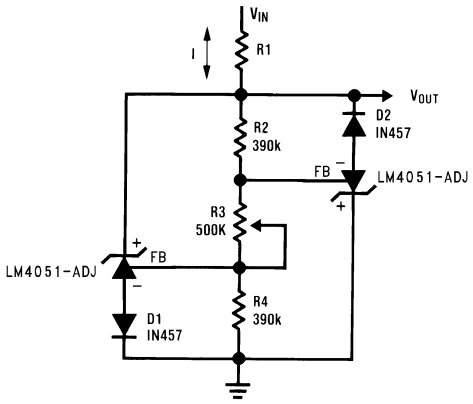


FIGURE 8. Bidirectional Adjustable Clamp ±18V to ±2.4V

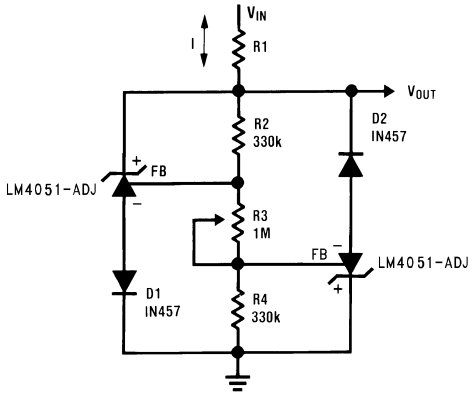


FIGURE 9. Bidirectional Adjustable Clamp ±2.4V to ±6V

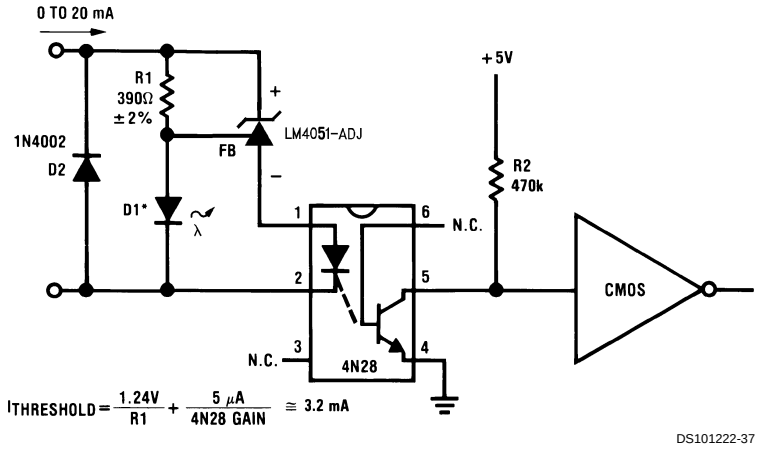


FIGURE 10. Simple Floating Current Detector

Typical Applications (Continued)

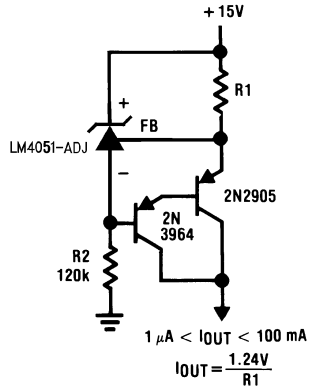


FIGURE 11. Current Source

Note 11: *D1 can be any LED, V_F = 1.5V to 2.2V at 3 mA. D1 may act as an indicator. D1 will be on if $I_{THRESHOLD}$ falls below the threshold current, except with I = O.

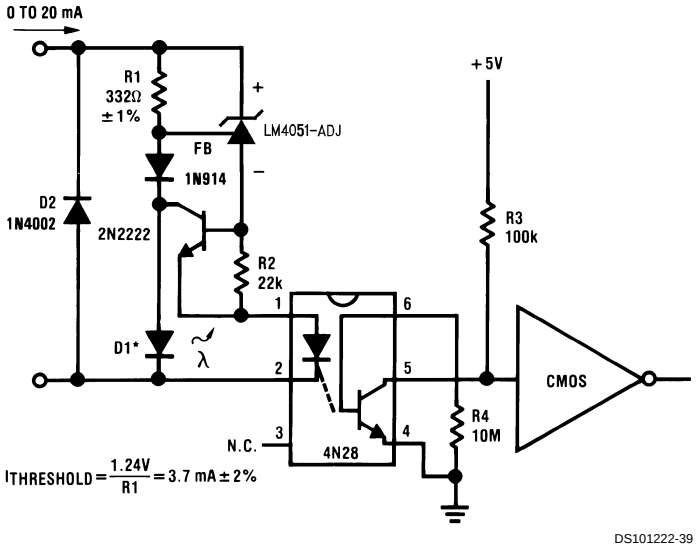
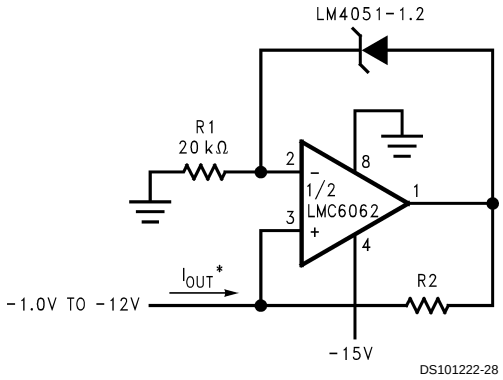


FIGURE 12. Precision Floating Current Detector

Typical Applications (Continued)



$$*I_{OUT} = \frac{1.2V}{R2}$$

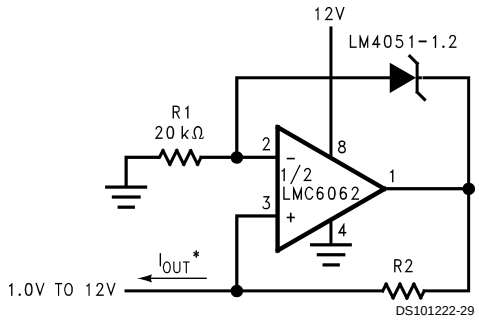
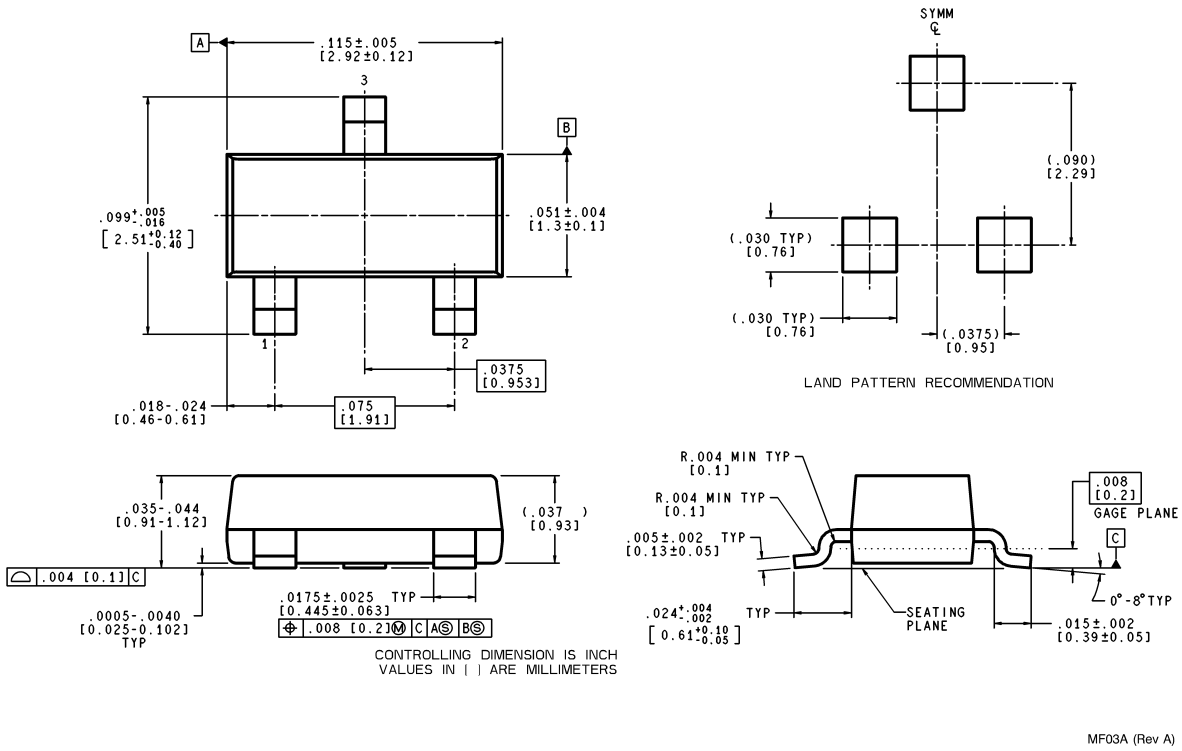


FIGURE 13. Precision 1 µA to 1 mA Current Sources

Physical Dimensions inches (millimeters) unless otherwise noted



MF03A (Rev A)

Plastic Surface Mount Package (M3)
NS Package Number MF03A
(JEDEC Registration TO-236AB)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National Semiconductor

November 2000

LM61
2.7V, SOT-23 or TO-92 Temperature Sensor

General Description

The LM61 is a precision integrated-circuit temperature sensor that can sense a −30˚C to +100˚C temperature range while operating from a single +2.7V supply. The LM61's output voltage is linearly proportional to Celsius (Centigrade) temperature (+10 mV/˚C) and has a DC offset of +600 mV. The offset allows reading negative temperatures without the need for a negative supply. The nominal output voltage of the LM61 ranges from +300 mV to +1600 mV for a −30˚C to +100˚C temperature range. The LM61 is calibrated to provide accuracies of ±2.0˚C at room temperature and ±3˚C over the full −25˚C to +85˚C temperature range.

The LM61's linear output, +600 mV offset, and factory calibration simplify external circuitry required in a single supply environment where reading negative temperatures is required. Because the LM61's quiescent current is less than 125 µA, self-heating is limited to a very low 0.2˚C in still air. Shutdown capability for the LM61 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates.

Features

- Calibrated linear scale factor of +10 mV/˚C
- Rated for full −30˚ to +100˚C range
- Suitable for remote applications

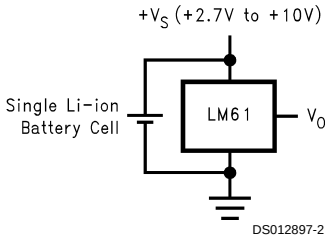
Applications

- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

Key Specifications

Accuracy at 25˚C	±2.0 or ±3.0˚C (max)
Accuracy for −30˚C to +100˚C	±4.0˚C (max)
Accuracy for −25˚C to +85˚C	±3.0˚C (max)
Temperature Slope	+10 mV/˚C
Power Supply Voltage Range	+2.7V to +10V
Current Drain @ 25˚C	125 µA (max)
Nonlinearity	±0.8˚C (max)
Output Impedance	800 Ω (max)

Typical Application



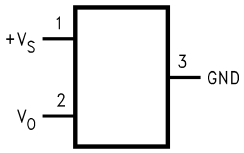
V_O = (+10 mV/˚C x T ˚C) + 600 mV

Temperature (T)	Typical V_O
+100˚C	+1600 mV
+85˚C	+1450 mV
+25˚C	+850 mV
0˚C	+600 mV
−25˚C	+350 mV
−30˚C	+300 mV

FIGURE 1. Full-Range Centigrade Temperature Sensor (−30˚C to +100˚C) Operating from a Single Li-Ion Battery Cell

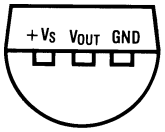
Connection Diagrams

SOT-23



Top View
See NS Package Number MA03B

TO-92



Top View
See NS Package Number Z03A

Ordering Information

Order Number	Device Marking	Supplied In	Accuracy Over Specified Temperature Range (˚C)	Specified Temperature Range	Package Type
LM61BIM3	T1B	1000 Units on Tape and Reel	± 3	−25˚C to +85˚C	SOT-23
LM61BIM3X	T1B	3000 Units on Tape and Reel			
LM61CIM3	T1C	1000 Units on Tape and Reel	± 4	−30˚C to +100˚C	
LM61CIM3X	T1C	3000 Units on Tape and Reel			
LM61BIZ	LM61BIZ	Bulk	± 3	−25˚C to +85˚C	TO-92
LM61CIZ	LM61CIZ	Bulk	± 4	−30˚C to +100˚C	

Absolute Maximum Ratings (Note 1)

Supply Voltage	+12V to −0.2V
Output Voltage	($+V_S$ + 0.6V) to −0.6V
Output Current	10 mA
Input Current at any pin (Note 2)	5 mA
Storage Temperature	−65˚C to +150˚C
Maximum Junction Temperature (T_{JMAX})	+125˚C
ESD Susceptibility (Note 3) :	
Human Body Model	2500V
Machine Model	250V
Lead Temperature:	
TO-92 Package:	
Soldering (10 seconds)	+260˚C
SOT-23 Package (Note 4):	
Vapor Phase (60 seconds)	+215˚C
Infrared (15 seconds)	+220˚C

Operating Ratings (Note 1)

Specified Temperature Range:	$T_{MIN} \le T_A \le T_{MAX}$
LM61C	$-30˚C \le T_A \le +100˚C$
LM61B	$-25˚C \le T_A \le +85˚C$
Supply Voltage Range ($+V_S$)	+2.7V to +10V
Thermal Resistance, θ_{JA} (Note 5)	
SOT-23	450˚C/W
TO-92	180˚C/W

Electrical Characteristics

Unless otherwise noted, these specifications apply for $+V_S$ = +3.0 V_{DC}. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}** ; all other limits $T_A = T_J$ = 25˚C.

Parameter	Conditions	Typical (Note 6)	LM61B Limits (Note 7)	LM61C Limits (Note 7)	Units (Limit)
Accuracy (Note 8)			±2.0	±3.0	˚C (max)
			±3.0	**±4.0**	˚C (max)
Output Voltage at 0˚C		+600			mV
Nonlinearity (Note 9)			**±0.6**	**±0.8**	˚C (max)
Sensor Gain		+10	**+9.7**	**+9.6**	mV/˚C (min)
(Average Slope)			**+10.3**	**+10.4**	mV/˚C (max)
Output Impedance	+3.0V ≤ $+V_S$ ≤ +10V		**0.8**	**0.8**	kΩ (max)
	−30˚C ≤ T_A ≤ +85˚C, $+V_S$= +2.7V		**2.3**	**2.3**	kΩ (max)
	+85˚C ≤ T_A ≤ +100˚C, $+V_S$= +2.7V		**5**	**5**	kΩ (max)
Line Regulation (Note 10)	+3.0V ≤ $+V_S$ ≤ +10V		**±0.7**	**±0.7**	mV/V (max)
	+2.7V ≤ $+V_S$ ≤ +3.3V		**±5.7**	**±5.7**	mV (max)
Quiescent Current	+2.7V ≤ $+V_S$ ≤ +10V	82	125	125	µA (max)
			155	**155**	µA (max)
Change of Quiescent Current	+2.7V ≤ $+V_S$ ≤ +10V	±5			µA
Temperature Coefficient of Quiescent Current		0.2			µA/˚C
Long Term Stability (Note 11)	T_J=T_{MAX}=+100˚C, for 1000 hours	±0.2			˚C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: When the input voltage (V_I) at any pin exceeds power supplies (V_I < GND or V_I > $+V_S$), the current at that pin should be limited to 5 mA.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 5: The junction to ambient thermal resistance (θ_{JA}) is specified without a heat sink in still air.

Note 6: Typicals are at $T_J = T_A$ = 25˚C and represent most likely parametric norm.

Note 7: Limits are guaranteed to National’s AOQL (Average Outgoing Quality Level).

Note 8: Accuracy is defined as the error between the output voltage and +10 mV/˚C times the device’s case temperature plus 600 mV, at specified conditions of voltage, current, and temperature (expressed in ˚C).

Note 9: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device’s rated temperature range.

Note 10: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

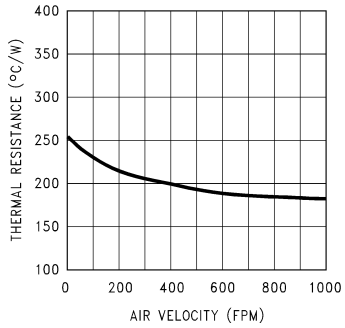
Electrical Characteristics (Continued)

Note 11: For best long-term stability, any precision circuit will give best results if the unit is aged at a warm temperature, and/or temperature cycled for at least 46 hours before long-term life test begins. This is especially true when a small (Surface-Mount) part is wave-soldered; allow time for stress relaxation to occur. The majority of the drift will occur in the first 1000 hours at elevated temperatures. The drift after 1000 hours will not continue at the first 1000 hour rate.

Typical Performance Characteristics

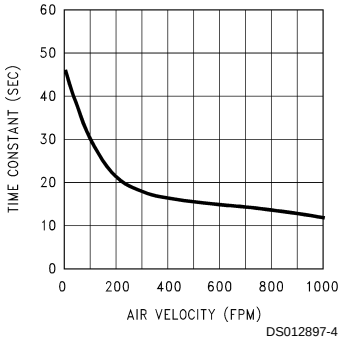
The LM61 in the SOT-23 package mounted to a printed circuit board as shown in *Figure 2* was used to generate the following thermal curves.

Thermal Resistance Junction to Air



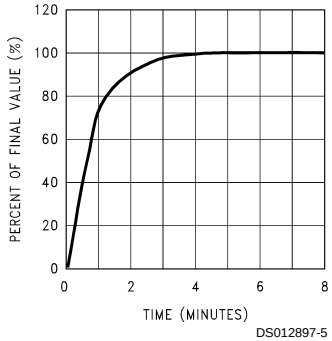
DS012897-3

Thermal Time Constant



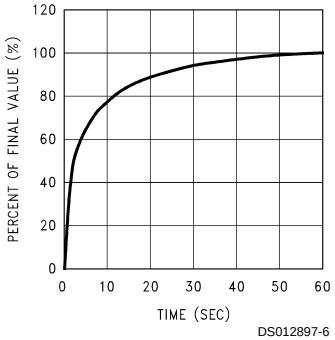
DS012897-4

Thermal Response in Still Air with Heat Sink



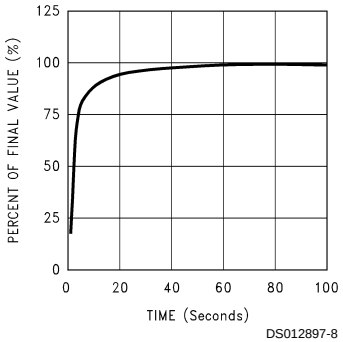
DS012897-5

Thermal Response in Stirred Oil Bath with Heat Sink



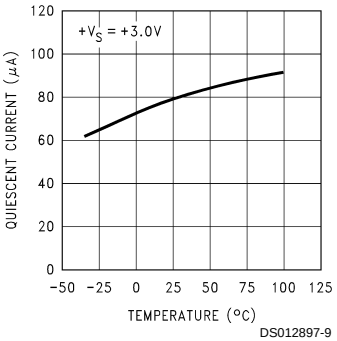
DS012897-6

Thermal Response in Still Air without a Heat Sink



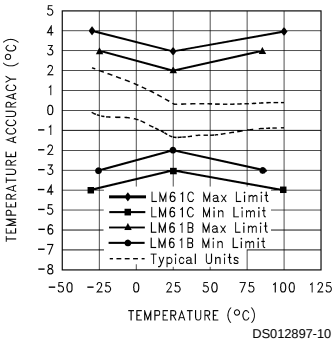
DS012897-8

Quiescent Current vs. Temperature



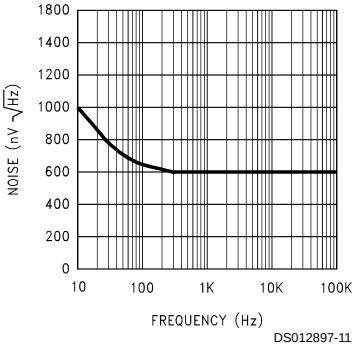
DS012897-9

Accuracy vs Temperature



DS012897-10

Noise Voltage

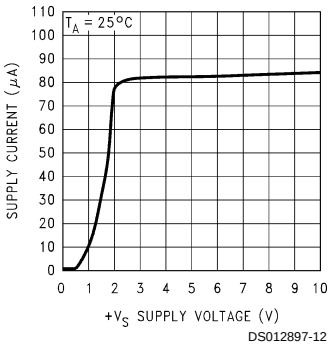


DS012897-11

Typical Performance Characteristics

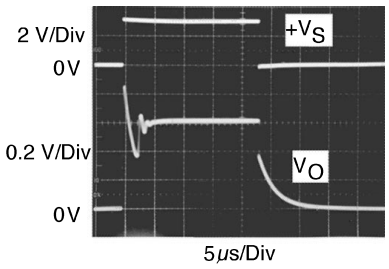
The LM61 in the SOT-23 package mounted to a printed circuit board as shown in *Figure 2* was used to generate the following thermal curves. (Continued)

Supply Voltage vs Supply Current

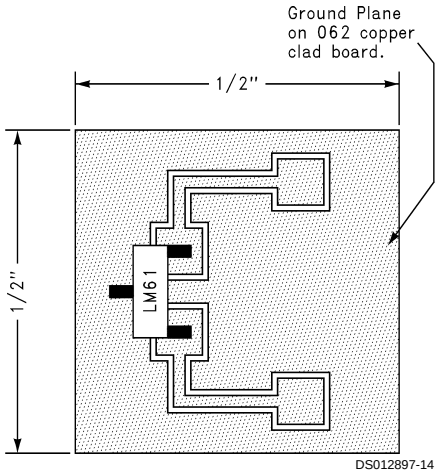


DS012897-12

Start-Up Response



DS012897-22



DS012897-14

FIGURE 2. Printed Circuit Board Used for Heat Sink to Generate All Curves. ½" Square Printed Circuit Board with 2 oz. Copper Foil or Similar.

1.0 Mounting

The LM61 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface. The temperature that the LM61 is sensing will be within about +0.2°C of the surface temperature that LM61's leads are attached to.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature measured would be at an intermediate temperature between the surface temperature and the air temperature.

To ensure good thermal conductivity the backside of the LM61 die is directly attached to the GND pin. The lands and traces to the LM61 will, of course, be part of the printed circuit board, which is the object whose temperature is being measured.

Alternatively, the LM61 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM61 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to ensure that moisture cannot corrode the LM61 or its connections.

The thermal resistance junction to ambient (θ_{JA}) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. For the LM61 the equation used to calculate the rise in the die temperature is as follows:

$$T_J = T_A + \theta_{JA} [(+V_S I_Q) + (+V_S - V_O) I_L]$$

where I_Q is the quiescent current and I_L is the load current on the output. Since the LM61's junction temperature is the actual temperature being measured care should be taken to minimize the load current that the LM61 is required to drive.

The table shown in *Figure 3* summarizes the rise in die temperature of the LM61 without any loading with a 3.3V supply, and the thermal resistance for different conditions.

1.0 Mounting (Continued)

	SOT-23* no heat sink		SOT-23** small heat fin		TO-92* no heat sink		TO-92*** small heat fin	
	θ_{JA} (°C/W)	$T_J - T_A$ (°C)	θ_{JA} (°C/W)	$T_J - T_A$ (°C)	θ_{JA} (°C/W)	$T_J - T_A$ (°C)	θ_{JA} (°C/W)	$T_J - T_A$ (°C)
Still air	450	0.26	260	0.13	180	0.09	140	0.07
Moving air			180	0.09	90	0.05	70	0.03

*Part soldered to 30 gauge wire.

**Heat sink used is ½" square printed circuit board with 2 oz. foil with part attached as shown in *Figure 2*.

***Part glued and leads soldered to 1″ square of 1/16″ printed circuit board with 2oz. foil or similar.

FIGURE 3. Temperature Rise of LM61 Due to Self-Heating and Thermal Resistance (θ_{JA})

2.0 Capacitive Loads

The LM61 handles capacitive loading well. Without any special precautions, the LM61 can drive any capacitive load as shown in *Figure 4*. Over the specified temperature range the LM61 has a maximum output impedance of 5 kΩ. In an extremely noisy environment it may be necessary to add some filtering to minimize noise pickup. It is recommended that 0.1 µF be added from $+V_S$ to GND to bypass the power supply voltage, as shown in *Figure 5*. In a noisy environment it may be necessary to add a capacitor from the output to ground. A 1 µF output capacitor with the 5 kΩ maximum output impedance will form a 32 Hz lowpass filter. Since the thermal time constant of the LM61 is much slower than the 5 ms time constant formed by the RC, the overall response time of the LM61 will not be significantly affected. For much larger capacitors this additional time lag will increase the overall response time of the LM61.

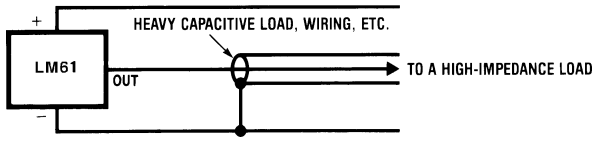


FIGURE 4. LM61 No Decoupling Required for Capacitive Load

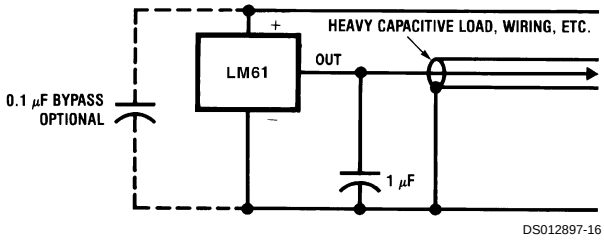


FIGURE 5. LM61 with Filter for Noisy Environment

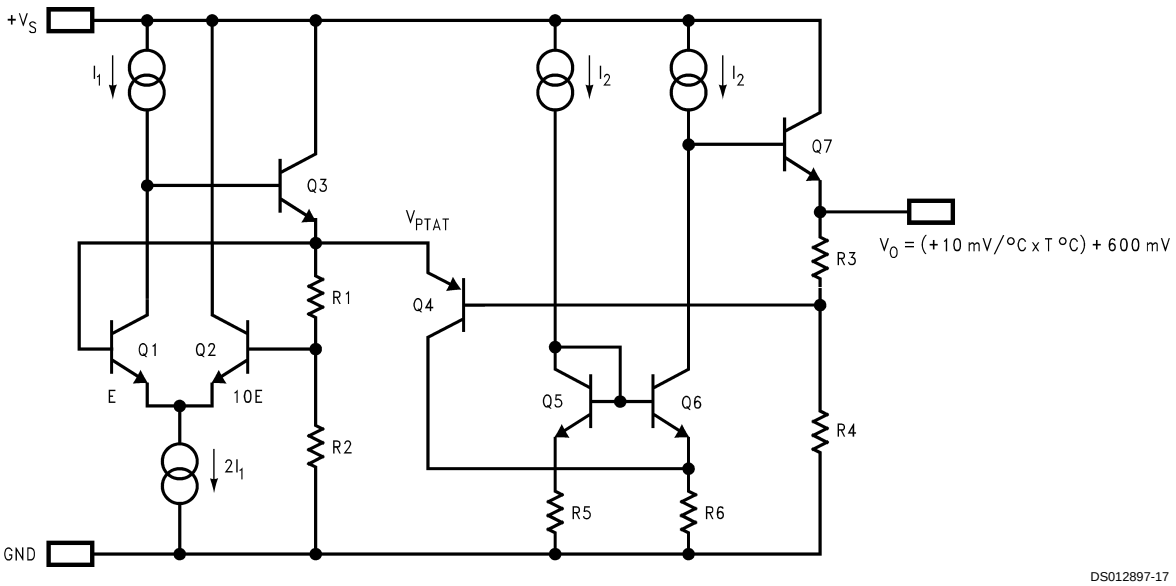
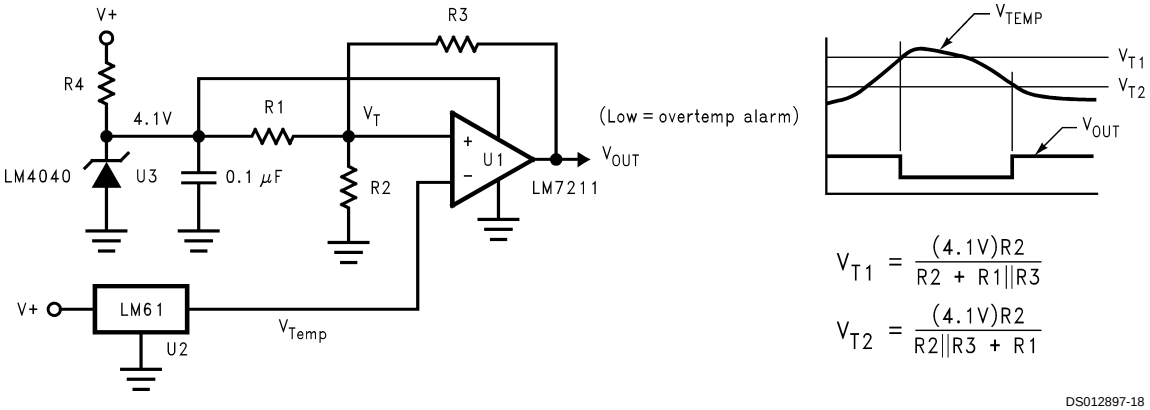


FIGURE 6. Simplified Schematic

3.0 Applications Circuits



$$V_{T1} = \frac{(4.1V)\,R2}{R2 + R1 \| R3}$$

$$V_{T2} = \frac{(4.1V)\,R2}{R2 \| R3 + R1}$$

FIGURE 7. Centigrade Thermostat

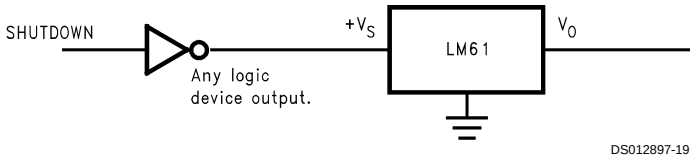
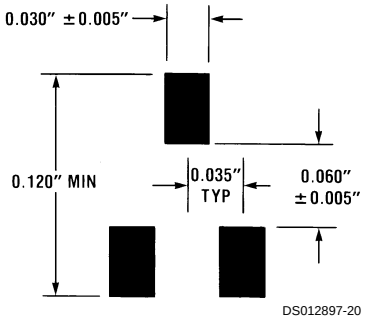
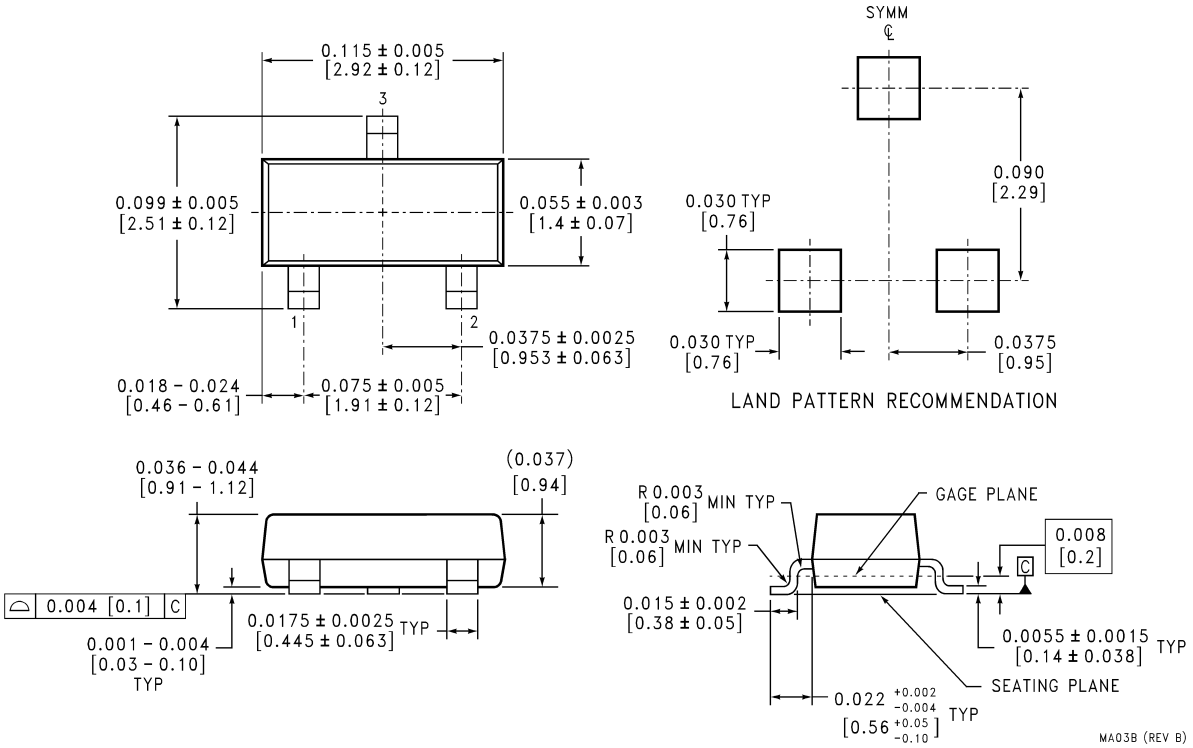


FIGURE 8. Conserving Power Dissipation with Shutdown

4.0 Recommended Solder Pads for SOT-23 Package

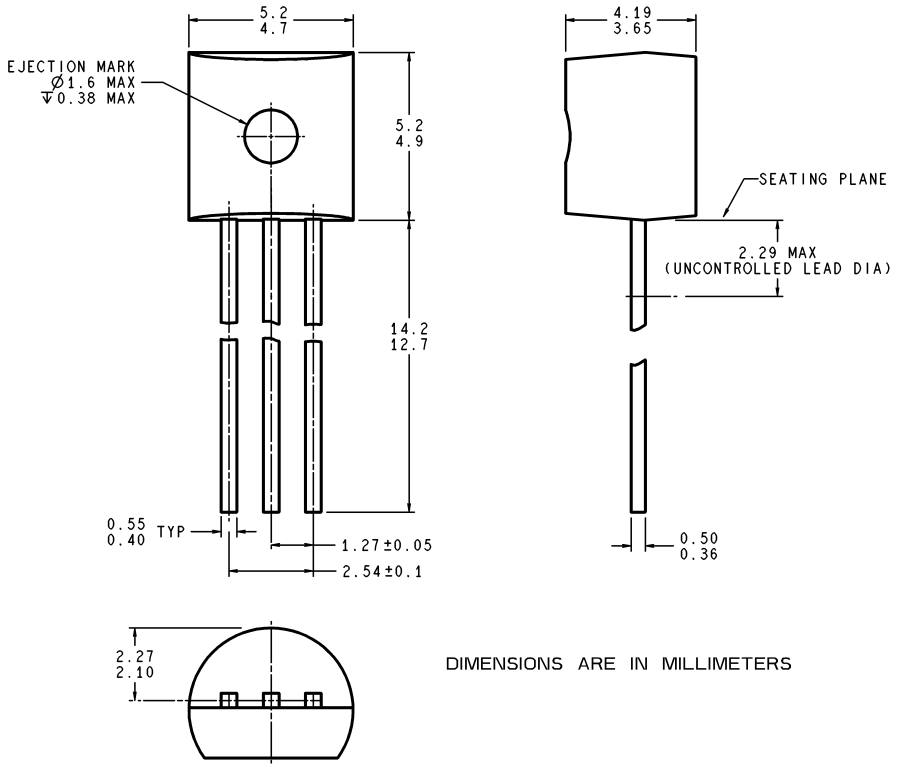


Physical Dimensions inches (millimeters) unless otherwise noted



SOT-23 Molded Small Outline Transistor Package (M3)
Order Number LM61BIM3 or LM61CIM3
NS Package Number MA03B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-92 Plastic Package (Z)
Order Number LM61BIZ or LM61CIZ
NS Package Number Z03A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com
www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

19-0410; Rev 3; 7/96

MAXIM

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

General Description

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E are low-power transceivers for RS-485 and RS-422 communications in harsh environments. Each driver output and receiver input is protected against ±15kV electrostatic discharge (ESD) shocks, without latchup. These parts contain one driver and one receiver. The MAX483E, MAX487E, MAX488E, and MAX489E feature reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, thus allowing error-free data transmission up to 250kbps. The driver slew rates of the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E are not limited, allowing them to transmit up to 2.5Mbps.

These transceivers draw as little as 120µA supply current when unloaded or when fully loaded with disabled drivers (see *Selection Table*). Additionally, the MAX481E, MAX483E, and MAX487E have a low-current shutdown mode in which they consume only 0.5µA. All parts operate from a single +5V supply.

Drivers are short-circuit current limited, and are protected against excessive power dissipation by thermal shutdown circuitry that places their outputs into a high-impedance state. The receiver input has a fail-safe feature that guarantees a logic-high output if the input is open circuit.

The MAX487E and MAX1487E feature quarter-unit-load receiver input impedance, allowing up to 128 transceivers on the bus. The MAX488E–MAX491E are designed for full-duplex communications, while the MAX481E, MAX483E, MAX485E, MAX487E, and MAX1487E are designed for half-duplex applications. For applications that are not ESD sensitive see the pin- and function-compatible MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487.

Applications

Low-Power RS-485 Transceivers

Low-Power RS-422 Transceivers

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local Area Networks

Features

- **ESD Protection: ±15kV—Human Body Model**
- **Slew-Rate Limited for Error-Free Data Transmission (MAX483E/487E/488E/489E)**
- **Low Quiescent Current:**
  120µA (MAX483E/487E/488E/489E)
  230µA (MAX1487E)
  300µA (MAX481E/485E/490E/491E)
- **-7V to +12V Common-Mode Input Voltage Range**
- **Three-State Outputs**
- **30ns Propagation Delays, 5ns Skew (MAX481E/485E/490E/491E/1487E)**
- **Full-Duplex and Half-Duplex Versions Available**
- **Allows up to 128 Transceivers on the Bus (MAX487E/MAX1487E)**
- **Current Limiting and Thermal Shutdown for Driver Overload Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX481ECPA	0°C to +70°C	8 Plastic DIP
MAX481ECSA	0°C to +70°C	8 SO
MAX481EEPA	-40°C to +85°C	8 Plastic DIP
MAX481EESA	-40°C to +85°C	8 SO

Ordering Information continued on last page.

Selection Table

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED	LOW-POWER SHUTDOWN	RECEIVER/ DRIVER ENABLE	QUIESCENT CURRENT (µA)	NUMBER OF TRANSMITTERS ON BUS	PIN COUNT
MAX481E	Half	2.5	No	Yes	Yes	300	32	8
MAX483E	Half	0.25	Yes	Yes	Yes	120	32	8
MAX485E	Half	2.5	No	No	Yes	300	32	8
MAX487E	Half	0.25	Yes	Yes	Yes	120	128	8
MAX488E	Full	0.25	Yes	No	No	120	32	8
MAX489E	Full	0.25	Yes	No	Yes	120	32	14
MAX490E	Full	2.5	No	No	No	300	32	8
MAX491E	Full	2.5	No	No	Yes	300	32	14
MAX1487E	Half	2.5	No	No	Yes	230	128	8

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 12V
Control Input Voltage ($\overline{RE}$, DE) ..... -0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI) ..... -0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (Y, Z; A, B) ..... -8V to +12.5V
Receiver Input Voltage (A, B) ..... -8V to +12.5V
Receiver Output Voltage (RO) ..... -0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ..800mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Ranges
MAX4_ _C_ _/MAX1487EC_ A ..... 0°C to +70°C
MAX4_ _E_ _/MAX1487EE_ A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Driver Output (no load)	V_{OD1}					5	V
Differential Driver Output (with load)	V_{OD2}	R = 50Ω (RS-422)		2			V
		R = 27Ω (RS-485), Figure 8		1.5		5	
Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R = 27Ω or 50Ω, Figure 8				3	V
Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	ΔV_{OD}	R = 27Ω or 50Ω, Figure 8				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±2	µA
Input Current (A, B)	I_{IN2}	DE = 0V; V_{CC} = 0V or 5.25V, all devices except MAX487E/MAX1487E	V_{IN} = 12V			1.0	mA
			V_{IN} = -7V			-0.8	
		MAX487E/MAX1487E, DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V			0.25	mA
			V_{IN} = -7V			-0.2	
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		-0.2		0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V			70		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = 200mV		3.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State (high impedance) Output Current at Receiver	I_{OZR}	0.4V ≤ V_O ≤ 2.4V				±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V, all devices except MAX487E/MAX1487E		12			kΩ
		-7V ≤ V_{CM} ≤ 12V, MAX487E/MAX1487E		48			kΩ

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
No-Load Supply Current (Note 3)	I_{CC}	MAX488E/MAX489E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				120	250	µA
		MAX490E/MAX491E, DE, DI, $\overline{RE}$ = 0V or V_{CC}				300	500	
		MAX481E/MAX485E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			500	900	
			DE = 0V			300	500	
		MAX1487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}			300	500	
			DE = 0V			230	400	
		MAX483E/MAX487E, $\overline{RE}$ = 0V or V_{CC}	DE = V_{CC}	MAX483E		350	650	
				MAX487E		250	400	
			DE = 0V			120	250	
Supply Current in Shutdown	I_{SHDN}	MAX481E/483E/487E, DE = 0V, $\overline{RE}$ = V_{CC}				0.5	10	µA
Driver Short-Circuit Current, V_O = High	I_{OSD1}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Driver Short-Circuit Current, V_O = Low	I_{OSD2}	-7V ≤ V_O ≤12V (Note 4)			35		250	mA
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}			7		95	mA
ESD Protection		A, B, Y and Z pins, tested using Human Body Model				±15		kV

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		10	40	60	ns
	t_{PHL}			10	40	60	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5	10	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	3	20	40	ns
			MAX490EC/E, MAX491EC/E	5	20	25	
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed			45	70	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed			45	70	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed			45	70	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed			45	70	ns
Receiver Input to Output	t_{PLH}, t_{PHL}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	MAX481E, MAX485E, MAX1487E	20	60	200	ns
			MAX490EC/E, MAX491EC/E	20	60	150	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF			5		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed			20	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed			20	50	ns
Maximum Data Rate	f_{MAX}			2.5			Mbps
Time to Shutdown	t_{SHDN}	MAX481E (Note 5)		50	200	600	ns

SWITCHING CHARACTERISTICS—MAX481E/MAX485E, MAX490E/MAX491E, MAX1487E (continued)

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 11 and 13, C_L = 100pF, S2 closed		45	100	ns
Driver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 11 and 13, C_L = 100pF, S1 closed		45	100	ns
Receiver Enable from Shutdown to Output High (MAX481E)	$t_{ZH(SHDN)}$	Figures 9 and 15, C_L = 15pF, S2 closed, A - B = 2V		225	1000	ns
Receiver Enable from Shutdown to Output Low (MAX481E)	$t_{ZL(SHDN)}$	Figures 9 and 15, C_L = 15pF, S1 closed, B - A = 2V		225	1000	ns

SWITCHING CHARACTERISTICS—MAX483E, MAX487E/MAX488E/MAX489E

(V_{CC} = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{PLH}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250	800	2000	ns
	t_{PHL}		250	800	2000	
Driver Output Skew to Output	t_{SKEW}	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		20	800	ns
Driver Rise or Fall Time	t_R, t_F	Figures 10 and 12, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
Driver Enable to Output High	t_{ZH}	Figures 11 and 13, C_L = 100pF, S2 closed	250		2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 11 and 13, C_L = 100pF, S1 closed	250		2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 11 and 13, C_L = 15pF, S1 closed	300		3000	ns
Driver Disable Time from High	t_{HZ}	Figures 11 and 13, C_L = 15pF, S2 closed	300		3000	ns
Receiver Input to Output	t_{PLH}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF	250		2000	ns
	t_{PHL}		250		2000	
$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew	t_{SKD}	Figures 10 and 14, R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF		100		ns
Receiver Enable to Output Low	t_{ZL}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Enable to Output High	t_{ZH}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Receiver Disable Time from Low	t_{LZ}	Figures 9 and 15, C_{RL} = 15pF, S1 closed		25	50	ns
Receiver Disable Time from High	t_{HZ}	Figures 9 and 15, C_{RL} = 15pF, S2 closed		25	50	ns
Maximum Data Rate	f_{MAX}	t_{PLH}, t_{PHL} < 50% of data period	250			kbps
Time to Shutdown	t_{SHDN}	MAX483E/MAX487E (Note 5)	50	200	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S2 closed			2000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 11 and 13, C_L = 100pF, S1 closed			2000	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S2 closed			2500	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	MAX483E/MAX487E, Figures 9 and 15, C_L = 15pF, S1 closed			2500	ns

NOTES FOR ELECTRICAL/SWITCHING CHARACTERISTICS

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 2: All typical specifications are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Supply current specification is valid for loaded transmitters when DE = 0V.

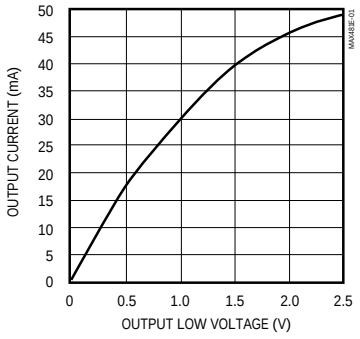
Note 4: Applies to peak current. See *Typical Operating Characteristics.*

Note 5: The MAX481E/MAX483E/MAX487E are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 600ns, the parts are guaranteed to have entered shutdown. See *Low-Power Shutdown Mode* section.

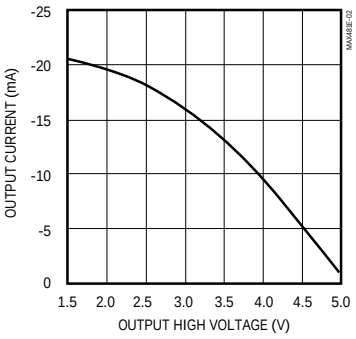
Typical Operating Characteristics

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

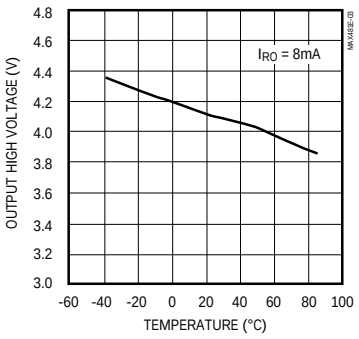
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



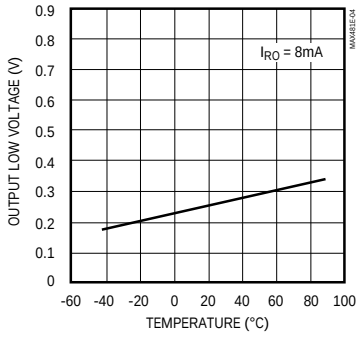
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



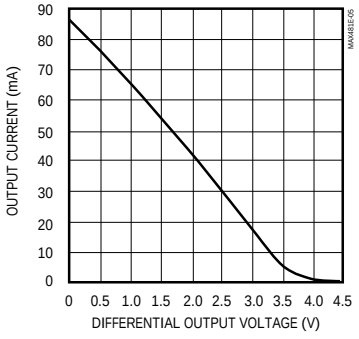
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE

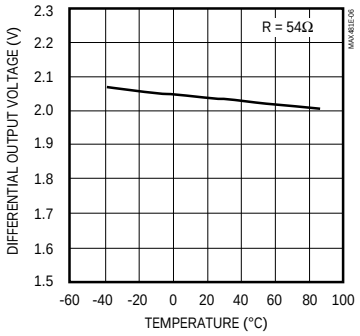


±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

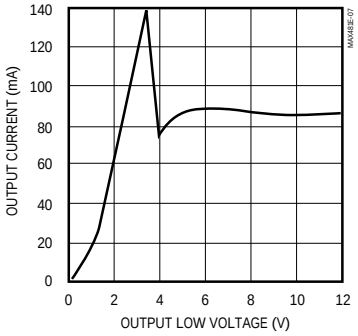
Typical Operating Characteristics (continued)

(V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

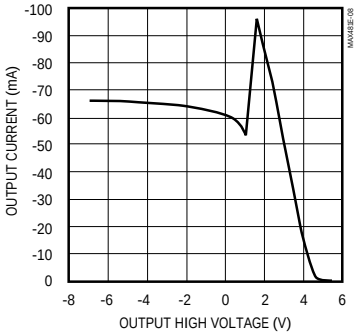
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



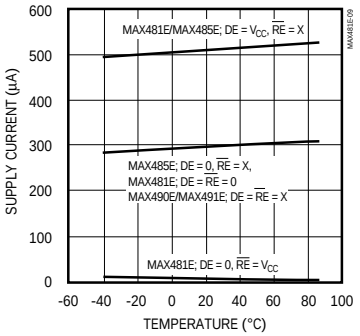
OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



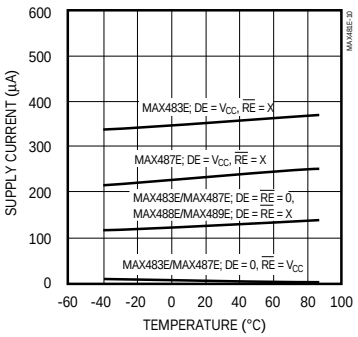
OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



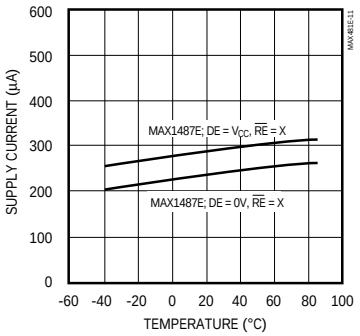
MAX481E/MAX485E/MAX490E/MAX491E SUPPLY CURRENT vs. TEMPERATURE



MAX483E/MAX487E–MAX489E SUPPLY CURRENT vs. TEMPERATURE



MAX1487E SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX481E/MAX483E MAX485E/MAX487E MAX1487E	MAX488E MAX490E	MAX489E MAX491E		
1	2	2	RO	Receiver Output: If A > B by 200mV, RO will be high; If A < B by 200mV, RO will be low.
2	—	3	$\overline{RE}$	Receiver Output Enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high.
3	—	4	DE	Driver Output Enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the driver outputs are enabled, the parts function as line drivers. While they are high impedance, they function as line receivers if $\overline{RE}$ is low.
4	3	5	DI	Driver Input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
5	4	6, 7	GND	Ground
—	5	9	Y	Noninverting Driver Output
—	6	10	Z	Inverting Driver Output
6	—	—	A	Noninverting Receiver Input and Noninverting Driver Output
—	8	12	A	Noninverting Receiver Input
7	—	—	B	Inverting Receiver Input and Inverting Driver Output
—	7	11	B	Inverting Receiver Input
8	1	14	V_{CC}	Positive Supply: $4.75V \le V_{CC} \le 5.25V$
—	—	1, 8, 13	N.C.	No Connect—not internally connected

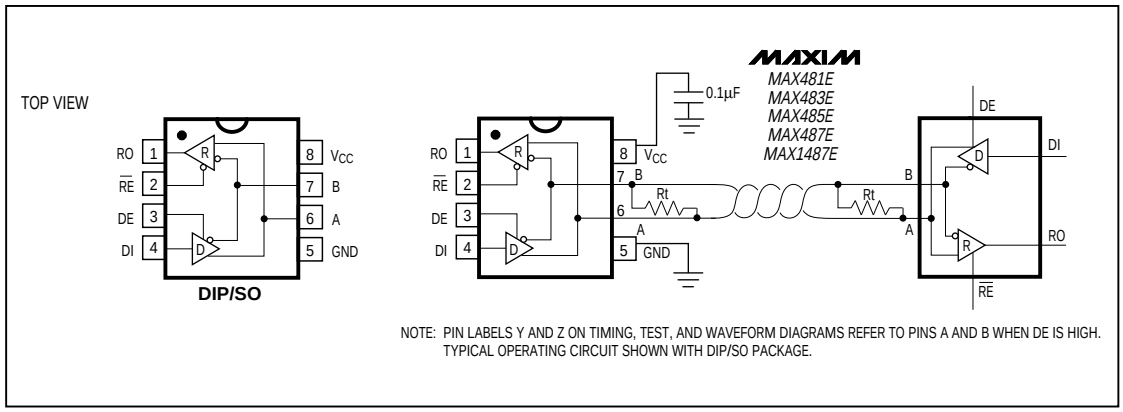


Figure 1. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Pin Configuration and Typical Operating Circuit

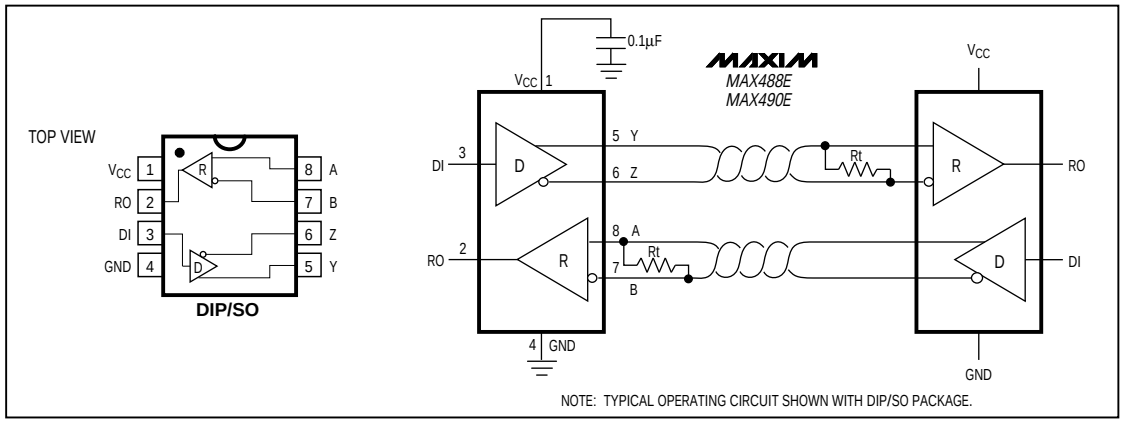


Figure 2. MAX488E/MAX490E Pin Configuration and Typical Operating Circuit

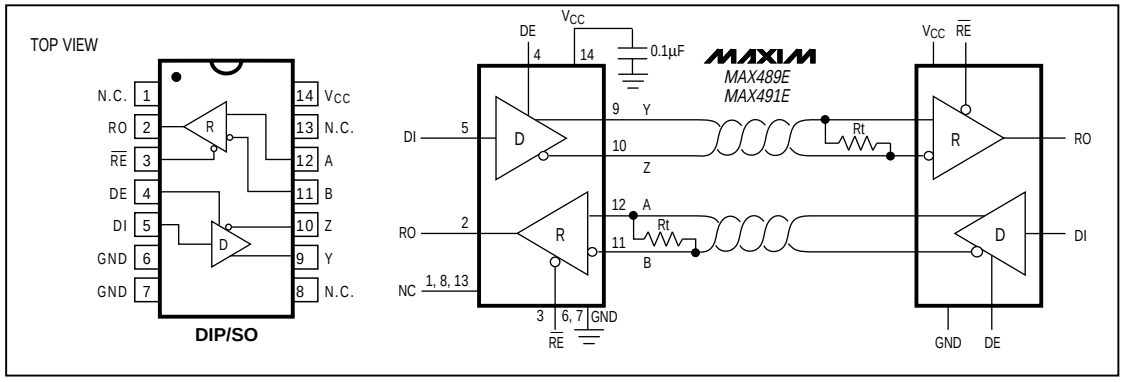


Figure 3. MAX489E/MAX491E Pin Configuration and Typical Operating Circuit

Function Tables (MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E)

Table 1. Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Table 2. Receiving

INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	≥ +0.2V	1
0	0	≤ -0.2V	0
0	0	Inputs open	1
1	0	X	High-Z*

X = Don't care
High-Z = High impedance
* Shutdown mode for MAX481E/MAX483E/MAX487E

Applications Information

The MAX481E/MAX483E/MAX485E/MAX487E–MAX491E and MAX1487E are low-power transceivers for RS-485 and RS-422 communications. These "E" versions of the MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 provide extra protection against ESD. The rugged MAX481E, MAX483E, MAX485E, MAX497E–MAX491E, and MAX1487E are intended for harsh environments where high-speed communication is important. These devices eliminate the need for transient suppressor diodes and the associated high capacitance loading. The standard (non-"E") MAX481, MAX483, MAX485, MAX487–MAX491, and MAX1487 are recommended for applications where cost is critical.

The MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E can transmit and receive at data rates up to 2.5Mbps, while the MAX483E, MAX487E, MAX488E, and MAX489E are specified for data rates up to 250kbps. The MAX488E–MAX491E are full-duplex transceivers, while the MAX481E, MAX483E, MAX487E, and MAX1487E are half-duplex. In addition, driver-enable (DE) and receiver-enable (RE) pins are included on the MAX481E, MAX483E, MAX485E, MAX487E, MAX489E, MAX491E, and MAX1487E. When disabled, the driver and receiver outputs are high impedance.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs have extra protection against static electricity. Maxim's engineers developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, Maxim's MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E keep working without latchup.

ESD protection can be tested in various ways; the transmitter outputs and receiver inputs of this product family are characterized for protection to ±15kV using the Human Body Model.

Other ESD test methodologies include IEC10004-2 contact discharge and IEC1000-4-2 air-gap discharge (formerly IEC801-2).

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test set-up, test methodology, and test results.

Human Body Model

Figure 4 shows the Human Body Model, and Figure 5 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC1000-4-2

The IEC1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits (Figure 6).

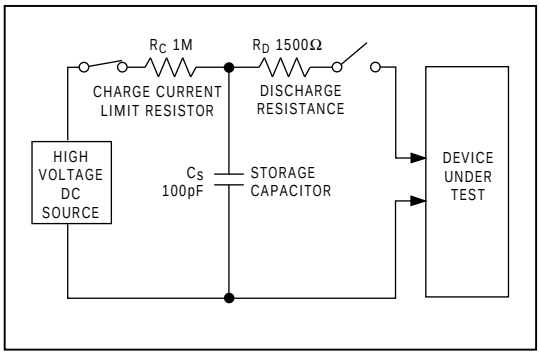


Figure 4. Human Body ESD Test Model

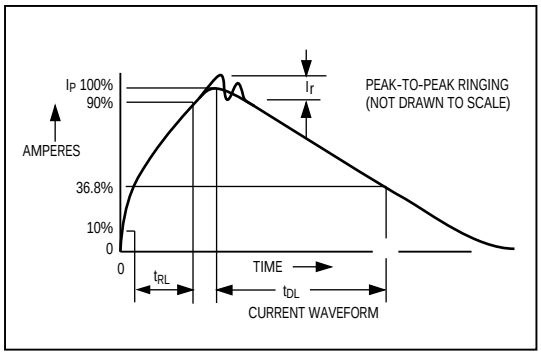


Figure 5. Human Body Model Current Waveform

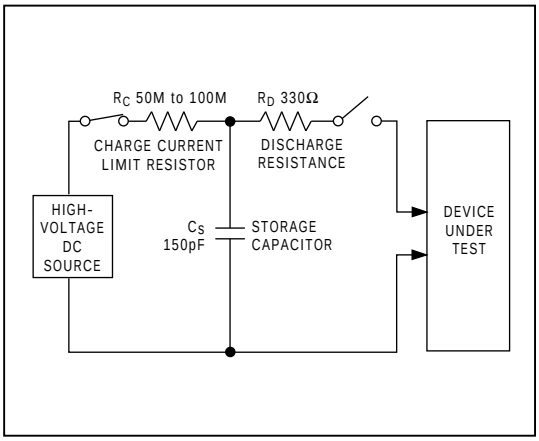


Figure 6. IEC1000-4-2 ESD Test Model

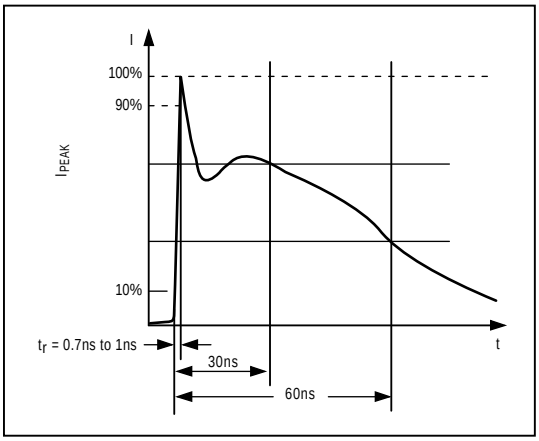


Figure 7. IEC1000-4-2 ESD Generator Current Waveform

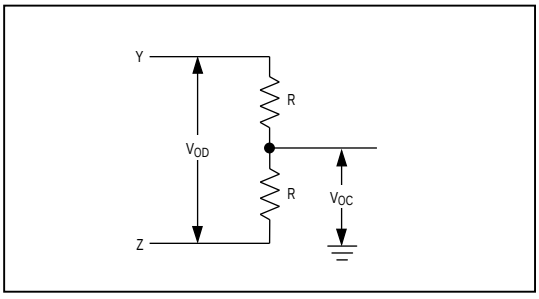


Figure 8. Driver DC Test Load

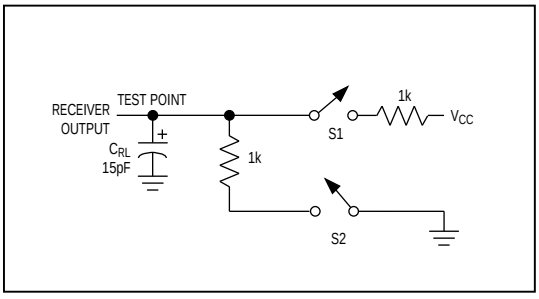


Figure 9. Receiver Timing Test Load

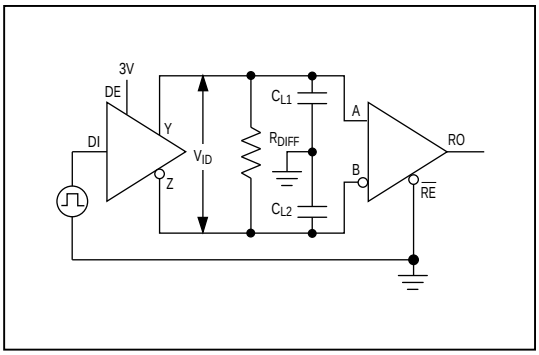


Figure 10. Driver/Receiver Timing Test Circuit

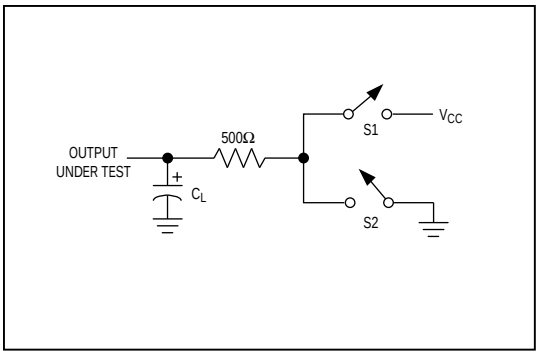


Figure 11. Driver Timing Test Load

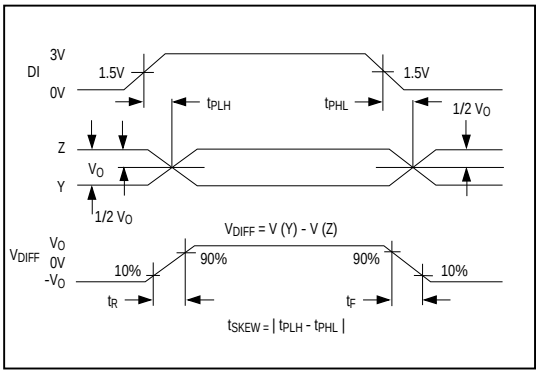


Figure 12. Driver Propagation Delays

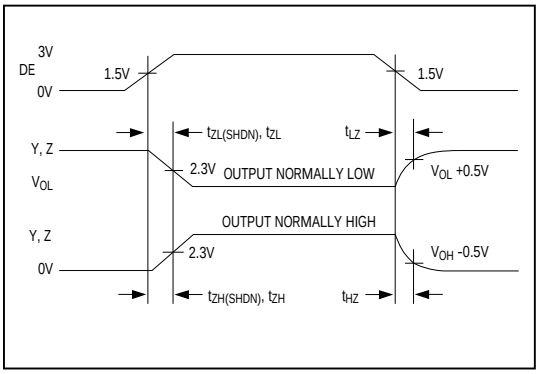


Figure 13. Driver Enable and Disable Times (except MAX488E and MAX490E)

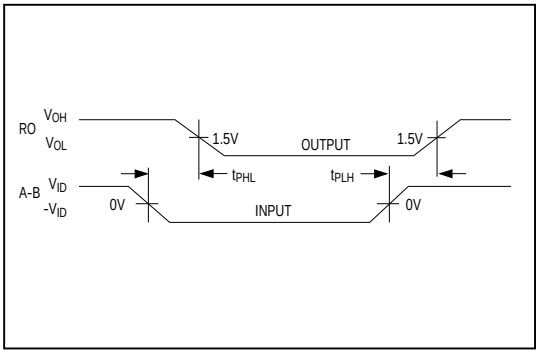


Figure 14. Receiver Propagation Delays

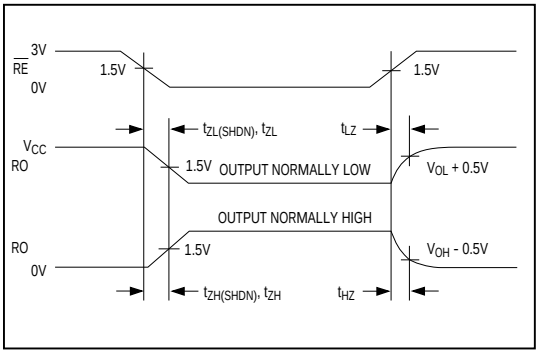


Figure 15. Receiver Enable and Disable Times (except MAX488E and MAX490E)

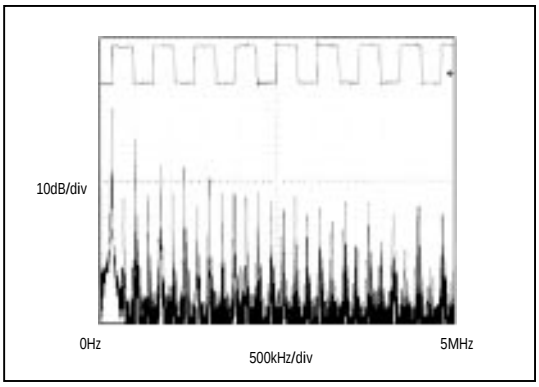


Figure 16. Driver Output Waveform and FFT Plot of MAX485E/MAX490E/MAX491E/MAX1487E Transmitting a 150kHz Signal

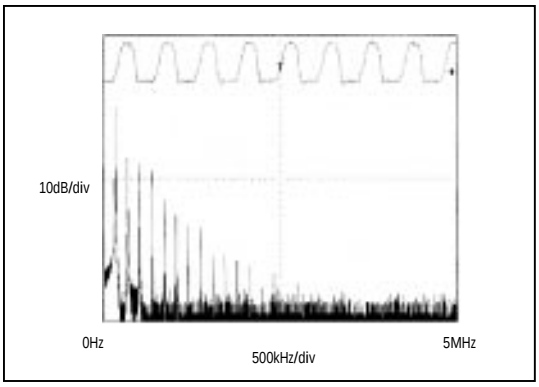


Figure 17. Driver Output Waveform and FFT Plot of MAX483E/MAX487E–MAX489E Transmitting a 150kHz Signal

The major difference between tests done using the Human Body Model and IEC1000-4-2 is higher peak current in IEC1000-4-2, because series resistance is lower in the IEC1000-4-2 model. Hence, the ESD withstand voltage measured to IEC1000-4-2 is generally lower than that measured using the Human Body Model. Figure 7 shows the current waveform for the 8kV IEC1000-4-2 ESD contact-discharge test.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. Its objective is to emulate the stress caused by contact that occurs with handling and assembly during manufacturing. Of course, all pins require this protection during manufacturing—not just inputs and outputs. Therefore, after PC board assembly, the Machine Model is less relevant to I/O ports.

MAX487E/MAX1487E: 128 Transceivers on the Bus

The 48kΩ, 1/4-unit-load receiver input impedance of the MAX487E and MAX1487E allows up to 128 transceivers on a bus, compared to the 1-unit load (12kΩ input impedance) of standard RS-485 drivers (32 transceivers maximum). Any combination of MAX487E/MAX1487E and other RS-485 transceivers with a total of 32 unit loads or less can be put on the bus. The MAX481E, MAX483E, MAX485E, and MAX488E–MAX491E have standard 12kΩ receiver input impedance.

MAX483E/MAX487E/MAX488E/MAX489E: Reduced EMI and Reflections

The MAX483E and MAX487E–MAX489E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 16 shows the driver output waveform and its Fourier analysis of a 150kHz signal transmitted by a MAX481E, MAX485E, MAX490E, MAX491E, or MAX1487E. High-frequency harmonics with large amplitudes are evident. Figure 17 shows the same information displayed for a MAX483E, MAX487E, MAX488E, or MAX489E transmitting under the same conditions. Figure 17's high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

Low-Power Shutdown Mode (MAX481E/MAX483E/MAX487E)

A low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. The devices will not shut down unless both the driver and receiver are disabled. In shutdown, the devices typically draw only 0.5µA of supply current.

$\overline{RE}$ and DE may be driven simultaneously; the parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

For the MAX481E, MAX483E, and MAX487E, the t_{ZH} and t_{ZL} enable times assume the part was not in the low-power shutdown state (the MAX485E, MAX488E–MAX491E, and MAX1487E can not be shut down). The $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ enable times assume the parts were shut down (see *Electrical Characteristics*).

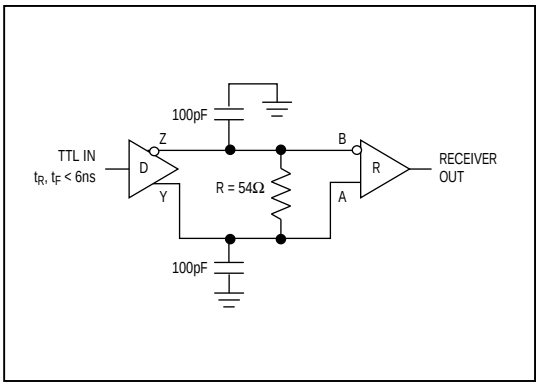


Figure 18. Receiver Propagation Delay Test Circuit

It takes the drivers and receivers longer to become enabled from the low-power shutdown state ($t_{ZH(SHDN)}$, $t_{ZL(SHDN)}$) than from the operating mode (t_{ZH}, t_{ZL}). (The parts are in operating mode if the $\overline{RE}$, DE inputs equal a logical 0,1 or 1,1 or 0, 0.)

Driver Output Protection

Excessive output current and power dissipation caused by faults or by bus contention are prevented by two mechanisms. A foldback current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). In addition, a thermal shutdown circuit forces the driver outputs into a high-impedance state if the die temperature rises excessively.

Propagation Delay

Many digital encoding schemes depend on the difference between the driver and receiver propagation delay times. Typical propagation delays are shown in Figures 19–22 using Figure 18's test circuit.

The difference in receiver delay times, t_{PLH} - t_{PHL}, is typically under 13ns for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and is typically less than 100ns for the MAX483E and MAX487E–MAX489E.

The driver skew times are typically 5ns (10ns max) for the MAX481E, MAX485E, MAX490E, MAX491E, and MAX1487E, and are typically 100ns (800ns max) for the MAX483E and MAX487E–MAX489E.

Typical Applications

The MAX481E, MAX483E, MAX485E, MAX487E–MAX491E, and MAX1487E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figures 25 and 26 show typical network application circuits. These parts can also be used as line repeaters, with cable lengths longer than 4000 feet.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX483E and MAX487E–MAX489E are more tolerant of imperfect termination. Bypass the V_{CC} pin with 0.1µF.

Isolated RS-485

For isolated RS-485 applications, see the MAX253 and MAX1480 data sheets.

Line Length vs. Data Rate

The RS-485/RS-422 standard covers line lengths up to 4000 feet. Figures 23 and 24 show the system differential voltage for the parts driving 4000 feet of 26AWG twisted-pair wire at 110kHz into 100Ω loads.

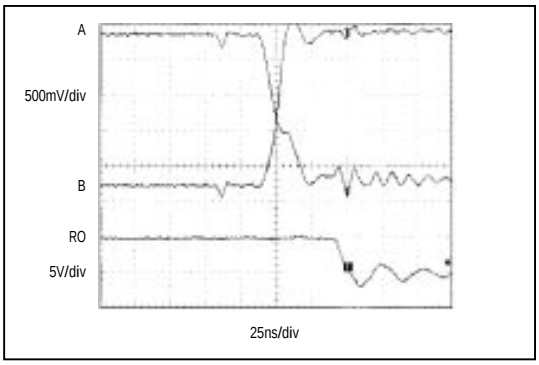


Figure 19. MAX481E/MAX485E/MAX490E/MAX1487E Receiver t_{PHL}

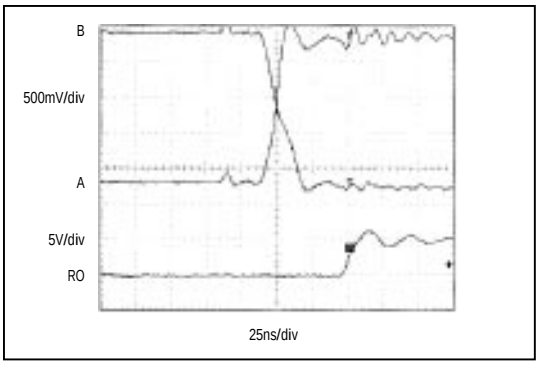


Figure 20. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E Receiver t_{PLH}

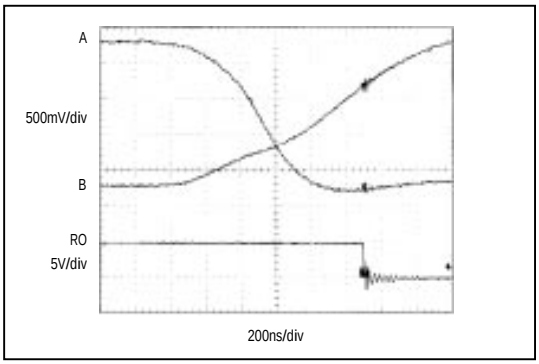


Figure 21. MAX483E/MAX487E–MAX489E Receiver t_{PHL}

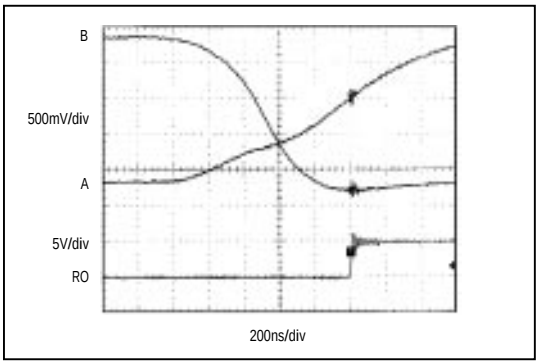


Figure 22. MAX483E/MAX487E–MAX489E Receiver t_{PLH}

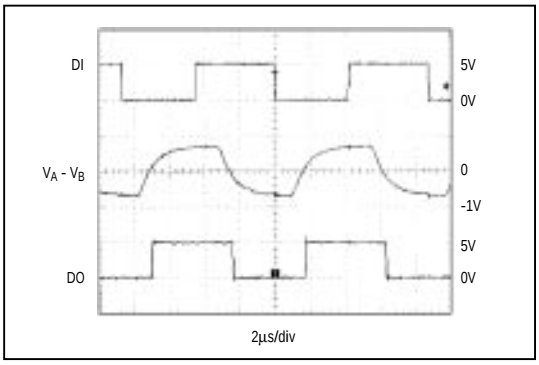


Figure 23. MAX481E/MAX485E/MAX490E/MAX491E/ MAX1487E System Differential Voltage at 110kHz Driving 4000ft of Cable

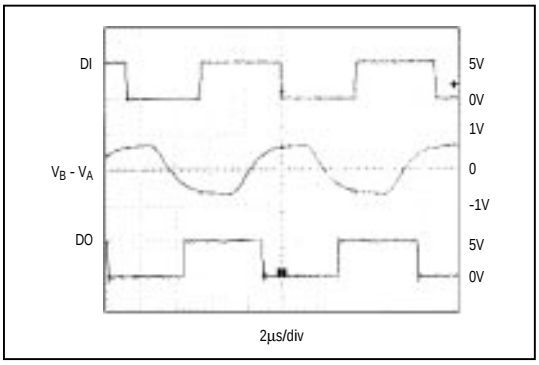


Figure 24. MAX483E/MAX1487E–MAX489E System Differential Voltage at 110kHz Driving 4000ft of Cable

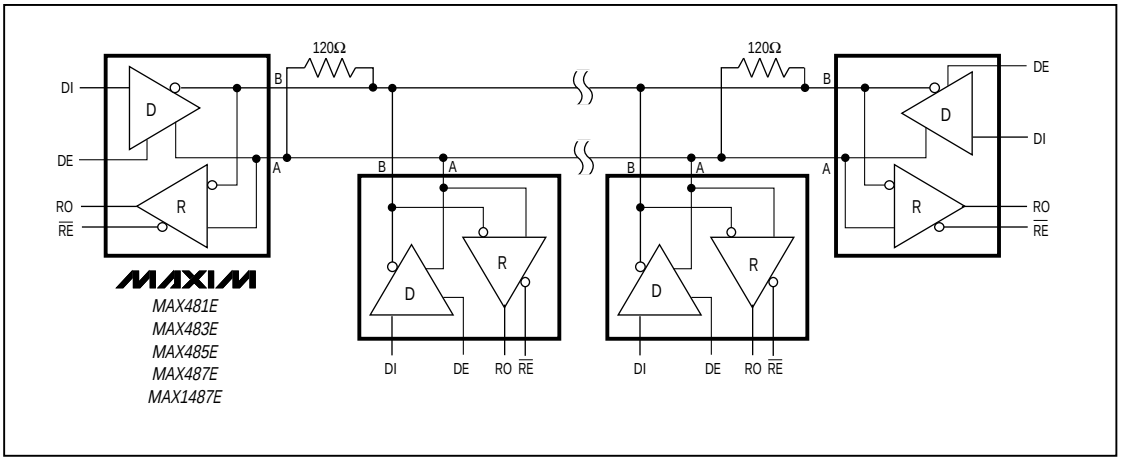


Figure 25. MAX481E/MAX483E/MAX485E/MAX487E/MAX1487E Typical Half-Duplex RS-485 Network

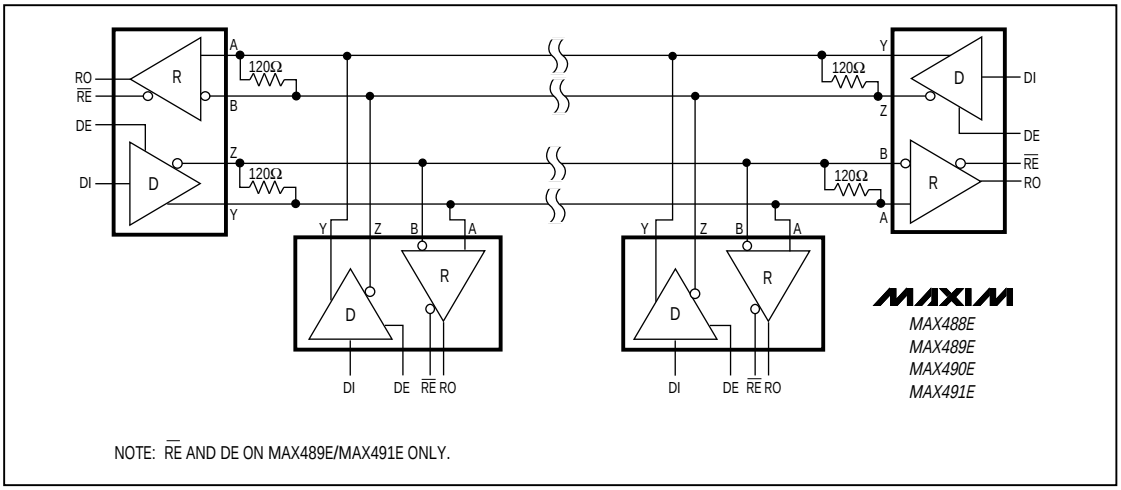


Figure 26. MAX488E–MAX491E Full-Duplex RS-485 Network

±15kV ESD-Protected, Slew-Rate-Limited, Low-Power, RS-485/RS-422 Transceivers

Ordering Information (continued)

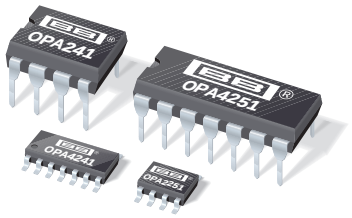
PART	TEMP. RANGE	PIN-PACKAGE
MAX483ECPA	0°C to +70°C	8 Plastic DIP
MAX483ECSA	0°C to +70°C	8 SO
MAX483EEPA	-40°C to +85°C	8 Plastic DIP
MAX483EESA	-40°C to +85°C	8 SO
MAX485ECPA	0°C to +70°C	8 Plastic DIP
MAX485ECSA	0°C to +70°C	8 SO
MAX485EEPA	-40°C to +85°C	8 Plastic DIP
MAX485EESA	-40°C to +85°C	8 SO
MAX487ECPA	0°C to +70°C	8 Plastic DIP
MAX487ECSA	0°C to +70°C	8 SO
MAX487EEPA	-40°C to +85°C	8 Plastic DIP
MAX487EESA	-40°C to +85°C	8 SO
MAX488ECPA	0°C to +70°C	8 Plastic DIP
MAX488ECSA	0°C to +70°C	8 SO
MAX488EEPA	-40°C to +85°C	8 Plastic DIP
MAX488EESA	-40°C to +85°C	8 SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX489ECPD	0°C to +70°C	14 Plastic DIP
MAX489ECSD	0°C to +70°C	14 SO
MAX489EEPD	-40°C to +85°C	14 Plastic DIP
MAX489EESD	-40°C to +85°C	14 SO
MAX490ECPA	0°C to +70°C	8 Plastic DIP
MAX490ECSA	0°C to +70°C	8 SO
MAX490EEPA	-40°C to +85°C	8 Plastic DIP
MAX490EESA	-40°C to +85°C	8 SO
MAX491ECPD	0°C to +70°C	14 Plastic DIP
MAX491ECSD	0°C to +70°C	14 SO
MAX491EEPD	-40°C to +85°C	14 Plastic DIP
MAX491EESD	-40°C to +85°C	14 SO
MAX1487ECPA	0°C to +70°C	8 Plastic DIP
MAX1487ECSA	0°C to +70°C	8 SO
MAX1487EEPA	-40°C to +85°C	8 Plastic DIP
MAX1487EESA	-40°C to +85°C	8 SO

Chip Information

TRANSISTOR COUNT: 295

BURR-BROWN®



OPA241
OPA2241
OPA4241

OPA251
OPA2251
OPA4251

Single-Supply, *Micro*POWER OPERATIONAL AMPLIFIERS

OPA241 Family optimized for +5V supply.

OPA251 Family optimized for ±15V supply.

FEATURES

- ***Micro*POWER: I_Q = 25µA**
- **SINGLE-SUPPLY OPERATION**
- **RAIL-TO-RAIL OUTPUT (within 50mV)**
- **WIDE SUPPLY RANGE**
  Single Supply: +2.7V to +36V
  Dual Supply: ±1.35V to ±18V
- **LOW OFFSET VOLTAGE: ±250µV max**
- **HIGH COMMON-MODE REJECTION: 124dB**
- **HIGH OPEN-LOOP GAIN: 128dB**
- **SINGLE, DUAL, AND QUAD**

APPLICATIONS

- **BATTERY OPERATED INSTRUMENTS**
- **PORTABLE DEVICES**
- **MEDICAL INSTRUMENTS**
- **TEST EQUIPMENT**

DESCRIPTION

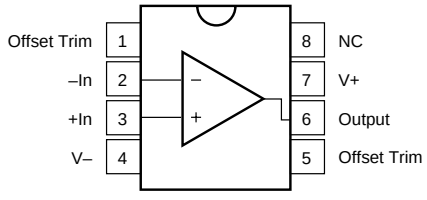
The OPA241 series and OPA251 series are specifically designed for battery powered, portable applications. In addition to very low power consumption (25µA), these amplifiers feature low offset voltage, rail-to-rail output swing, high common-mode rejection, and high open-loop gain.

The OPA241 series is optimized for operation at low power supply voltage while the OPA251 series is optimized for high power supplies. Both can operate from either single (+2.7V to +36V) or dual supplies (±1.35V to ±18V). The input common-mode voltage range extends 200mV below the negative supply—ideal for single-supply applications.

They are unity-gain stable and can drive large capacitive loads. Special design considerations assure that these products are easy to use. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±250µV max) is so low, user adjustment is usually not required. However, external trim pins are provided for special applications (single versions only).

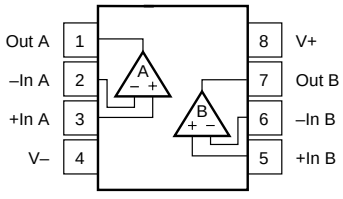
The OPA241 and OPA251 (single versions) are available in standard 8-pin DIP and SO-8 surface-mount packages. The OPA2241 and OPA2251 (dual versions) come in 8-pin DIP and SO-8 surface-mount packages. The OPA4241 and OPA4251 (quad versions) are available in 14-pin DIP and SO-14 surface-mount packages. All are fully specified from –40°C to +85°C and operate from –55°C to +125°C.

OPA241, OPA251



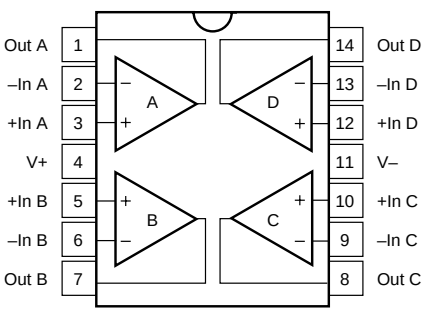
8-Pin DIP, SO-8

OPA2241, OPA2251



8-Pin DIP, SO-8

OPA4241, OPA4251



14-Pin DIP, SO-14

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1406B
Printed in U.S.A. October, 1998
SBOS075

SPECIFICATIONS: V_S = 2.7V to 5V

At T_A = +25°C, R_L = 100kΩ connected to V_S/2, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA MIN	TYP(1)	MAX	OPA251UA, PA OPA2251UA, PA OPA4251UA, PA MIN	TYP(1)	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±50	±250		±100		µV
T_A = –40°C to +85°C				**±100**	**±400**		**±130**		µV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to +85°C**		**±0.4**			**±0.6**		µV/°C
vs Power Supply	PSRR	V_S = 2.7V to 36V		3	30		*	*	µV/V
T_A = –40°C to +85°C		V_S = 2.7V to 36V			**30**			*	µV/V
Channel Separation (dual, quad)				0.3			*		µV/V
INPUT BIAS CURRENT									
Input Bias Current(2)	I_B			–4	–20		*		nA
T_A = –40°C to +85°C					**–25**				nA
Input Offset Current	I_{OS}			±0.1	±2		*		nA
T_A = –40°C to +85°C					**±2**				nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				1			*		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			45			*		nV/√Hz
Current Noise Density, f = 1kHz	i_n			40			*		fA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}		–0.2		(V+) –0.8				V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –0.2V to (V+) –0.8V	80	106			*		dB
T_A = –40°C to +85°C		V_{CM} = 0V to (V+) –0.8V	**80**						dB
INPUT IMPEDANCE									
Differential				10^7 || 2			*		Ω || pF
Common-Mode				10^9 || 4			*		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, V_O = (V–)+100mV to (V+)–100mV	100	120			*		dB
T_A = –40°C to +85°C		R_L = 100kΩ, V_O = (V–)+100mV to (V+)–100mV	**100**						dB
		R_L = 10kΩ, V_O = (V–)+200mV to (V+)–200mV	100	120			*		dB
T_A = –40°C to +85°C		R_L = 10kΩ, V_O = (V–)+200mV to (V+)–200mV	**100**						dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW			35			*		kHz
Slew Rate	SR	V_S = 5V, G = 1		0.01			*		V/µs
Overload Recovery Time		V_{IN} • G = V_S		60			*		µs
OUTPUT									
Voltage Output Swing from Rail(3)	V_O	R_L = 100kΩ to V_S/2, A_{OL} ≥ 70dB		50			*		mV
		R_L = 100kΩ to V_S/2, A_{OL} ≥ 100dB		75	100		*		mV
T_A = –40°C to +85°C		R_L = 100kΩ to V_S/2, A_{OL} ≥ 100dB			**100**				mV
		R_L = 10kΩ to V_S/2, A_{OL} ≥ 100dB		100	200		*		mV
T_A = –40°C to +85°C		R_L = 10kΩ to V_S/2, A_{OL} ≥ 100dB			**200**				mV
Short-Circuit Current	I_{SC}								
Single Versions				–24/+4			*		mA
Dual, Quad Versions				–30/+4			*		mA
Capacitive Load Drive	C_{LOAD}	See Typical Curve					*		
POWER SUPPLY									
Specified Voltage Range	V_S			+2.7 to +5			*		V
Operating Voltage Range		**T_A = –40°C to +85°C**	**+2.7**		**+36**	*		*	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±25	±30		*		µA
T_A = –40°C to +85°C		I_O = 0			**±36**				µA
TEMPERATURE RANGE									
Specified Range			–40		+85	*		*	°C
Operating Range			–55		+125	*		*	°C
Storage Range			–55		+125	*		*	°C
Thermal Resistance	θ_{JA}								
8-Pin DIP				100			*		°C/W
SO-8 Surface Mount				150			*		°C/W
14-Pin DIP				80			*		°C/W
SO-14 Surface Mount				100			*		°C/W

* Specifications the same as OPA241UA, PA.

NOTES: (1) V_S = +5V. (2) The negative sign indicates input bias current flows out of the input terminals. (3) Output voltage swings are measured between the output and power supply rails.

SPECIFICATIONS: $V_S = \pm 15V$

At T_A = +25°C, R_L = 100kΩ connected to ground, unless otherwise noted.
Boldface limits apply over the specified temperature range, T_A = –40°C to +85°C.

PARAMETER		CONDITION	OPA241UA, PA OPA2241UA, PA OPA4241UA, PA MIN	TYP	MAX	OPA251UA, PA OPA2251UA, PA OPA4251UA, PA MIN	TYP	MAX	UNITS
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}			±100			±50	±250	µV
T_A = –40°C to +85°C				**±150**			**±100**	**±300**	µV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to +85°C**		**±0.6**			**±0.5**		µV/°C
vs Power Supply	PSRR	V_S = ±1.35V to ±18V		*	*		3	30	µV/V
T_A = –40°C to +85°C		V_S = ±1.35V to ±18V			*			**30**	µV/V
Channel Separation (dual, quad)				*			0.3		µV/V
INPUT BIAS CURRENT									
Input Bias Current[1]	I_B			*			–4	–20	nA
T_A = –40°C to +85°C								**–25**	nA
Input Offset Current	I_{OS}			*			±0.1	±2	nA
T_A = –40°C to +85°C								**±2**	nA
NOISE									
Input Voltage Noise, f = 0.1Hz to 10Hz				*			1		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			*			45		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			*			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}					(V–) –0.2		(V+) –0.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15.2V to 14.2V		*		100	124		dB
T_A = –40°C to +85°C		V_{CM} = –15V to 14.2V				**100**			dB
INPUT IMPEDANCE									
Differential				*			10^7 || 2		Ω || pF
Common-Mode				*			10^9 || 4		Ω || pF
OPEN-LOOP GAIN									
Open-Loop Voltage Gain	A_{OL}	R_L = 100kΩ, V_O = –14.75V to +14.75V		*		100	128		dB
T_A = –40°C to +85°C		R_L = 100kΩ, V_O = –14.75V to +14.75V				**100**			dB
		R_L = 20kΩ, V_O = –14.7V to +14.7V		*		100	128		dB
T_A = –40°C to +85°C		R_L = 20kΩ, V_O = –14.7V to +14.7V				**100**			dB
FREQUENCY RESPONSE									
Gain-Bandwidth Product	GBW			*			35		kHz
Slew Rate	SR	G = 1		*			0.01		V/µs
Overload Recovery Time		V_{IN} • G = V_S		*			60		µs
OUTPUT									
Voltage Output Swing from Rail[2]	V_O	R_L = 100kΩ, A_{OL} ≥ 70dB		*			50		mV
		R_L = 100kΩ, A_{OL} ≥ 100dB		*			75	250	mV
T_A = –40°C to +85°C		R_L = 100kΩ, A_{OL} ≥ 100dB						**250**	mV
		R_L = 20kΩ, A_{OL} ≥ 100dB		*			100	300	mV
T_A = –40°C to +85°C		R_L = 20kΩ, A_{OL} ≥ 100dB						**300**	mV
Short-Circuit Current	I_{SC}								
Single Versions				*			–21/+4		mA
Dual Versions				*			–50/+4		mA
Capacitive Load Drive	C_{LOAD}			*			See Typical Curve		
POWER SUPPLY									
Specified Voltage Range	V_S			*			±15		V
Operating Voltage Range		**T_A = –40°C to +85°C**	*		*	**±1.35**		**±18**	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		*			±27	±38	µA
T_A = –40°C to +85°C		I_O = 0						**±45**	µA
TEMPERATURE RANGE									
Specified Range			*		*	–40		+85	°C
Operating Range			*		*	–55		+125	°C
Storage Range			*		*	–55		+125	°C
Thermal Resistance	θ_{JA}								
8-Pin DIP				*			100		°C/W
SO-8 Surface Mount				*			150		°C/W
14-Pin DIP				*			80		°C/W
SO-14 Surface Mount				*			100		°C/W

* Specifications the same as OPA251UA, PA.

NOTES: (1) The negative sign indicates input bias current flows out of the input terminals. (2) Output voltage swings are measured between the output and power supply rails.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Voltage[2]	(V–) –0.5V to (V+) +0.5V
Output Short Circuit to Ground[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more that 0.5V beyond the supply rails should be current-limited to 5mA or less. (3) One amplifier per package.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	SPECIFIED VOLTAGE	OPERATING VOLTAGE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]	SPECIFICATION TEMPERATURE RANGE
OPA241 SERIES					
Single					
OPA241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Dual					
OPA2241PA	2.7V to 5V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA2241UA	2.7V to 5V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Quad					
OPA4241PA	2.7V to 5V	2.7V to 36V	14-Pin DIP	010	–40°C to +85°C
OPA4241UA	2.7V to 5V	2.7V to 36V	SO-14 Surface Mount	235	–40°C to +85°C
OPA251 SERIES					
Single					
OPA251PA	±15V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Dual					
OPA2251PA	±15V	2.7V to 36V	8-Pin DIP	006	–40°C to +85°C
OPA2251UA	±15V	2.7V to 36V	SO-8 Surface Mount	182	–40°C to +85°C
Quad					
OPA4251PA	±15V	2.7V to 36V	14-Pin DIP	010	–40°C to +85°C
OPA4251UA	±15V	2.7V to 36V	SO-14 Surface Mount	235	–40°C to +85°C

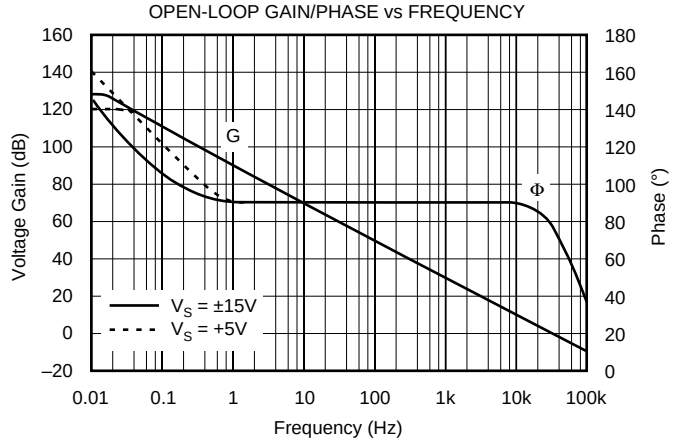
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

TYPICAL PERFORMANCE CURVES

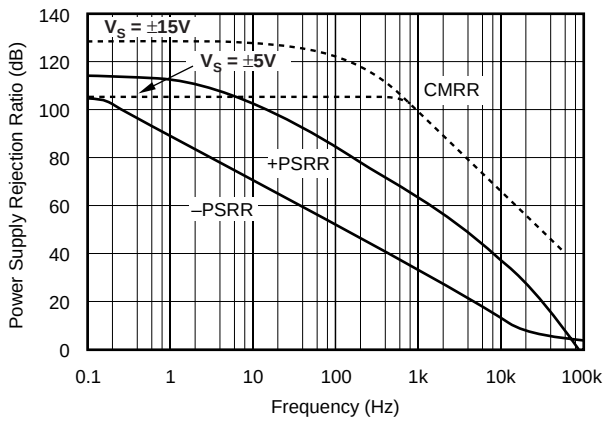
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

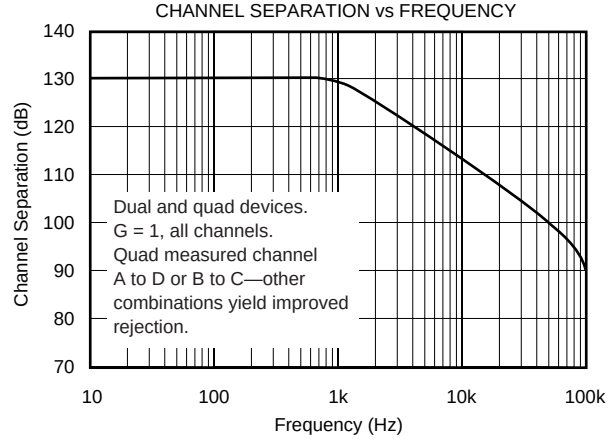
OPEN-LOOP GAIN/PHASE vs FREQUENCY



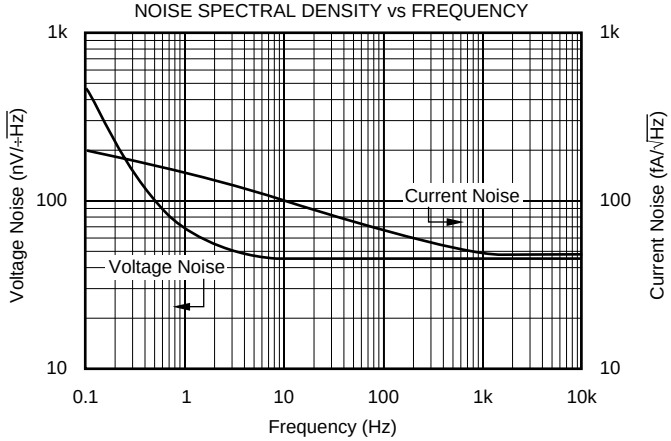
POWER SUPPLY and COMMON-MODE REJECTION RATIO vs FREQUENCY



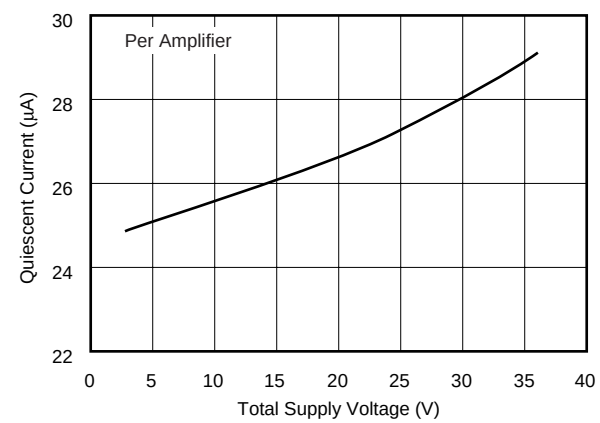
CHANNEL SEPARATION vs FREQUENCY



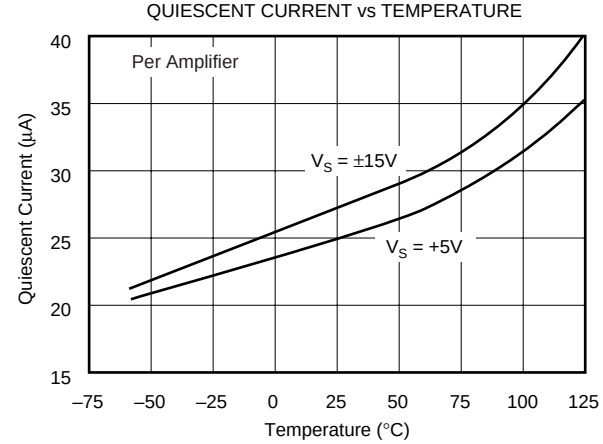
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



QUIESCENT CURRENT vs SUPPLY VOLTAGE



QUIESCENT CURRENT vs TEMPERATURE

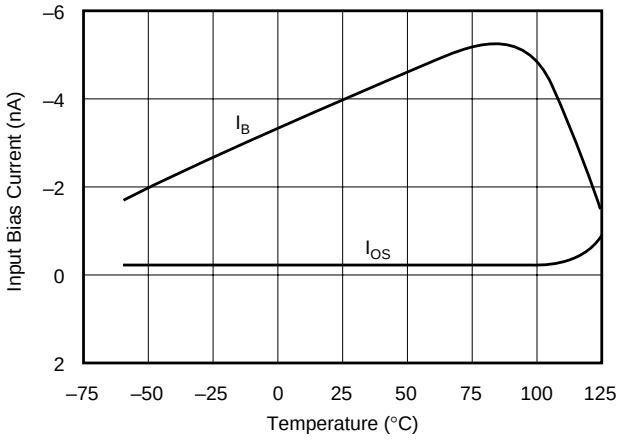


TYPICAL PERFORMANCE CURVES (CONT)

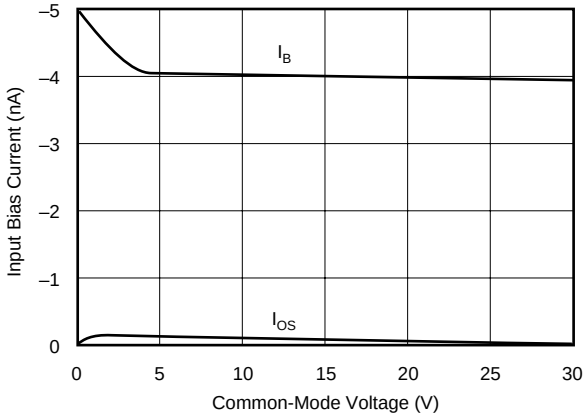
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

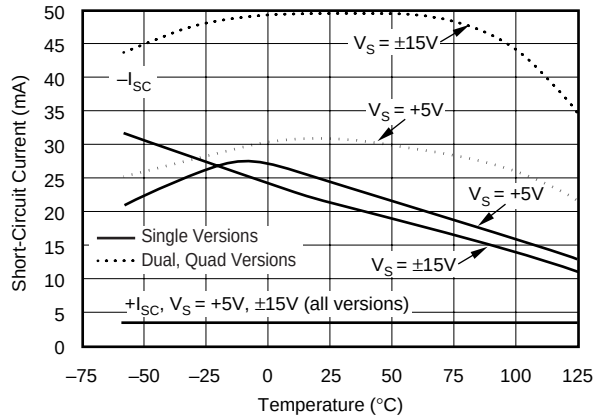
INPUT BIAS CURRENT vs TEMPERATURE



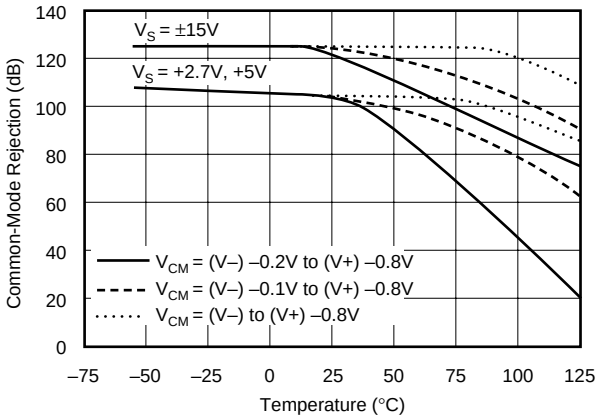
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



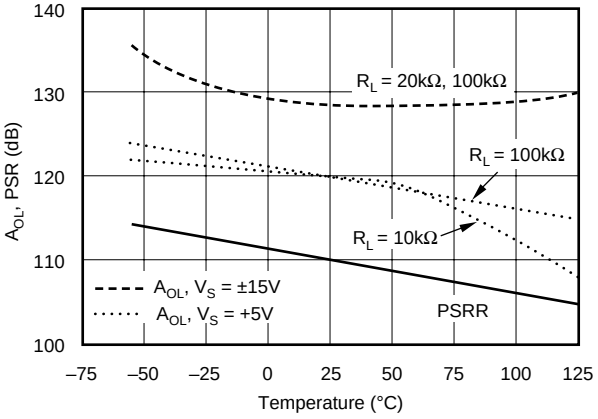
SHORT-CIRCUIT CURRENT vs TEMPERATURE



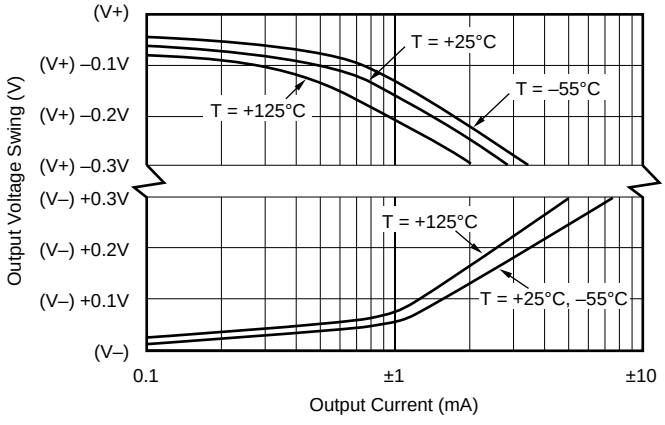
COMMON-MODE REJECTION vs TEMPERATURE



OPEN-LOOP GAIN AND POWER
SUPPLY REJECTION vs TEMPERATURE



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

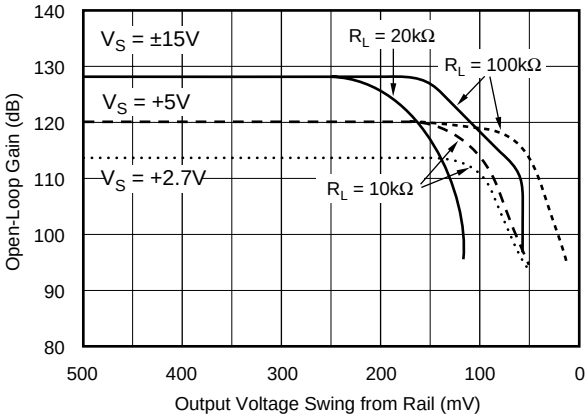


TYPICAL PERFORMANCE CURVES (CONT)

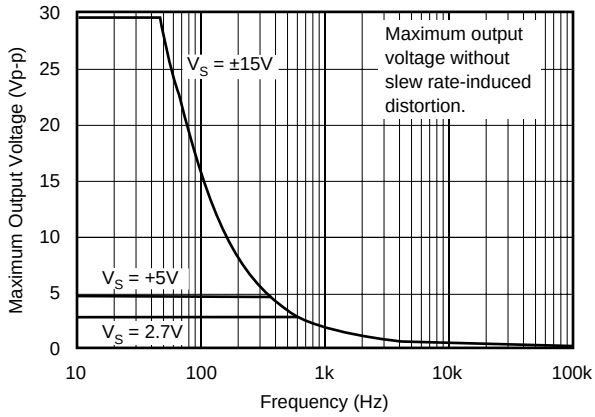
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S = ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

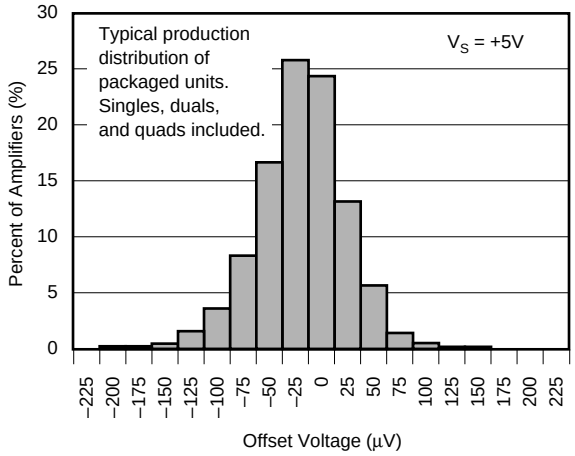
OPEN-LOOP GAIN vs OUTPUT VOLTAGE SWING



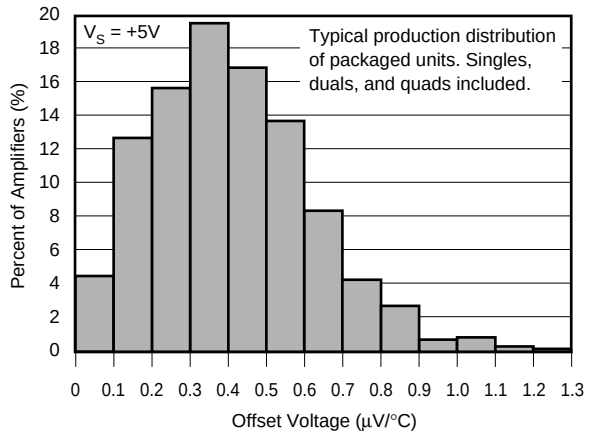
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



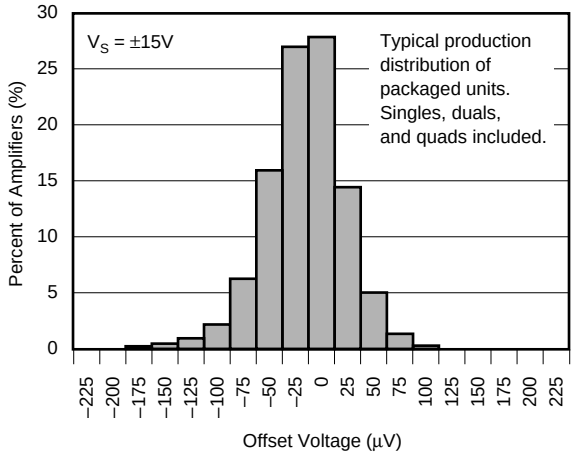
OPA241 SERIES OFFSET VOLTAGE PRODUCTION DISTRIBUTION



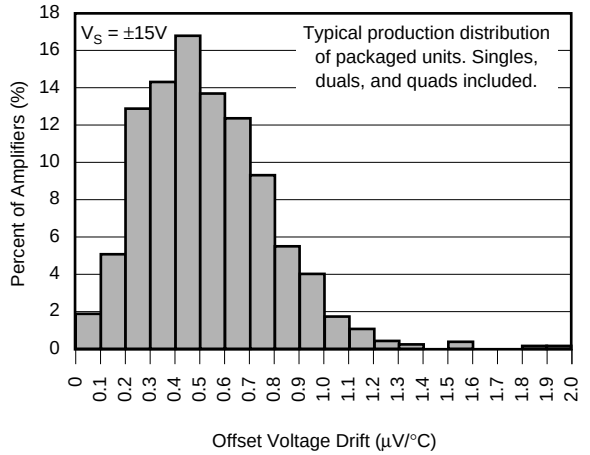
OPA241 SERIES OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



OPA251 SERIES OFFSET VOLTAGE PRODUCTION DISTRIBUTION



OPA251 SERIES OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

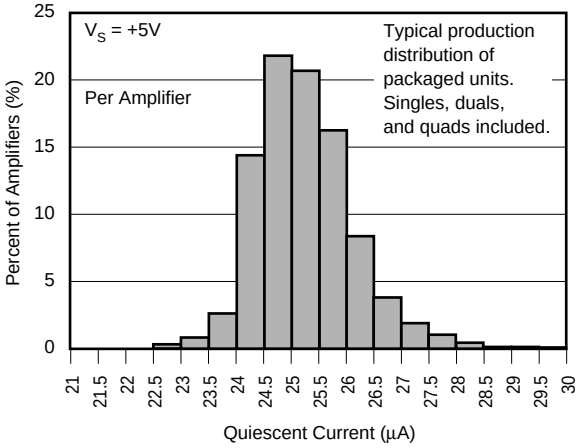


TYPICAL PERFORMANCE CURVES (CONT)

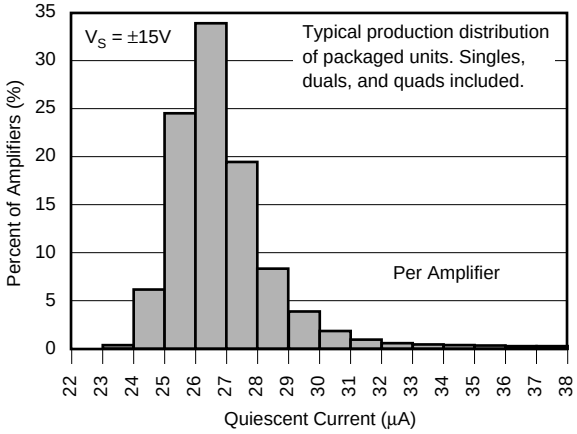
At T_A = +25°C, and R_L = 100kΩ connected to V_S/2 (ground for V_S ±15V), unless otherwise noted.

Curves apply to OPA241 and OPA251 unless specified.

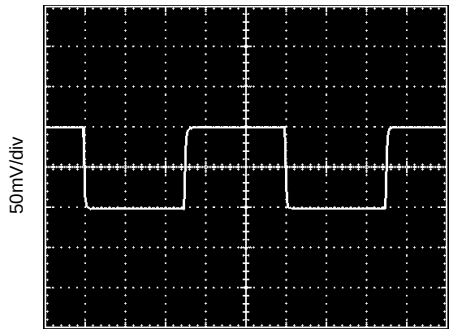
QUIESCENT CURRENT
PRODUCT DISTRIBUTION



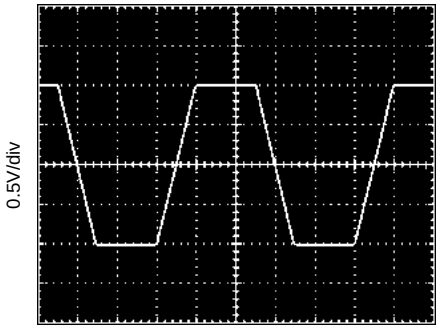
QUIESCENT CURRENT
PRODUCTION DISTRIBUTION



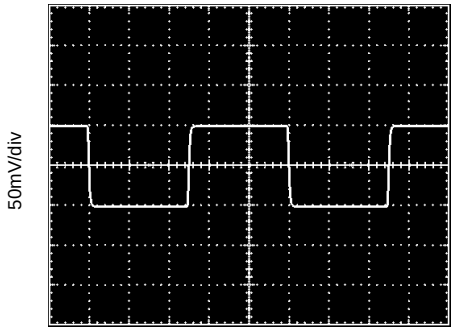
OPA241
SMALL-SIGNAL STEP RESPONSE
V_S = +5V, G = +1, R_L = 100kΩ, C_L = 100pF



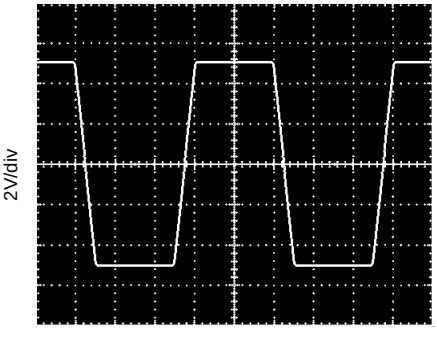
OPA241
LARGE-SIGNAL STEP RESPONSE
V_S = +5V, G + 1, R_L = 100kΩ, C_L = 100pF



OPA251
SMALL-SIGNAL STEP RESPONSE
V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF



OPA251
LARGE-SIGNAL STEP RESPONSE
V_S = ±15V, G = +1, R_L = 100kΩ, C_L = 500pF



APPLICATIONS INFORMATION

The OPA241 and OPA251 series are unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA241 series is laser-trimmed for low offset voltage and drift at low supply voltage (V_S = +5V). The OPA251 series is trimmed for ±15V operation. Both products operate over the full voltage range (+2.7V to +36V or ±1.35V to ±18V) with some compromises in offset voltage and drift performance. However, all other parameters have similar performance. Key parameters are guaranteed over the specified temperature range, –40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

OFFSET VOLTAGE TRIM

As mentioned previously, offset voltage of the OPA241 series is laser-trimmed at +5V. The OPA251 series is trimmed at ±15V. Because the initial offset is so low, user adjustment is usually not required. However, the OPA241 and OPA251 (single op amp versions) provide offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

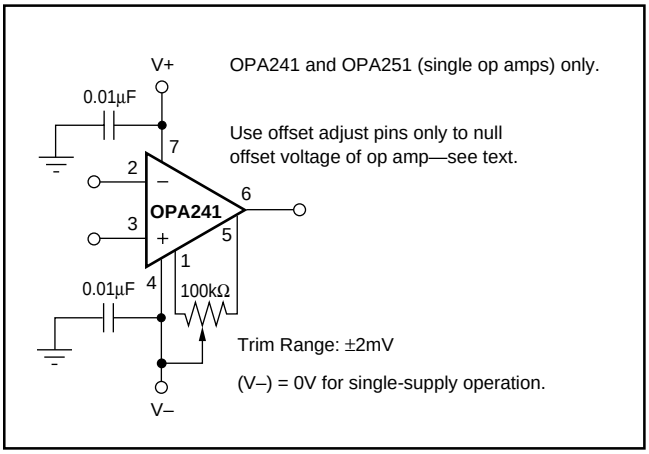


FIGURE 1. OPA241 and OPA251 Offset Voltage Trim Circuit.

CAPACITIVE LOAD AND STABILITY

The OPA241 series and OPA251 series can drive a wide range of capacitive loads. However, all op amps under certain conditions may be unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability.

Figures 2 and 3 show the regions where the OPA241 series and OPA251 series have the potential for instability. As shown, the unity gain configuration with low supplies is the most susceptible to the effects of capacitive load. With V_S = +5V, G = +1, and I_{OUT} = 0, operation remains stable with load capacitance up to approximately 200pF. Increasing supply voltage, output current, and/or gain significantly improves capacitive load drive. For example, increasing the supplies to ±15V and gain to 10 allows approximately 2700pF to be driven.

One method of improving capacitive load drive in the unity gain configuration is to insert a resistor inside the feedback loop as shown in Figure 4. This reduces ringing with large capacitive loads while maintaining dc accuracy. For example, with V_S = ±1.35V and R_S = 5kΩ, the OPA241 series and OPA251 series perform well with capacitive loads in excess of 1000pF. Without the series resistor, capacitive load drive is typically 200pF for these conditions. However, this method will result in a slight reduction of output voltage swing.

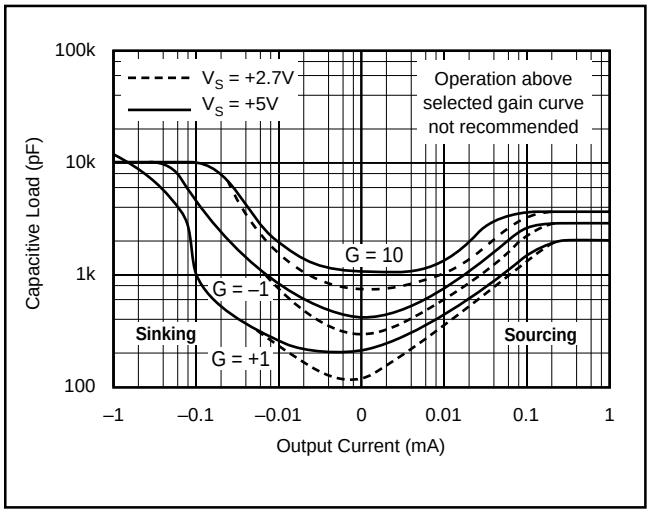


FIGURE 2. Stability—Capacitive Load versus Output Current for Low Supply Voltage.

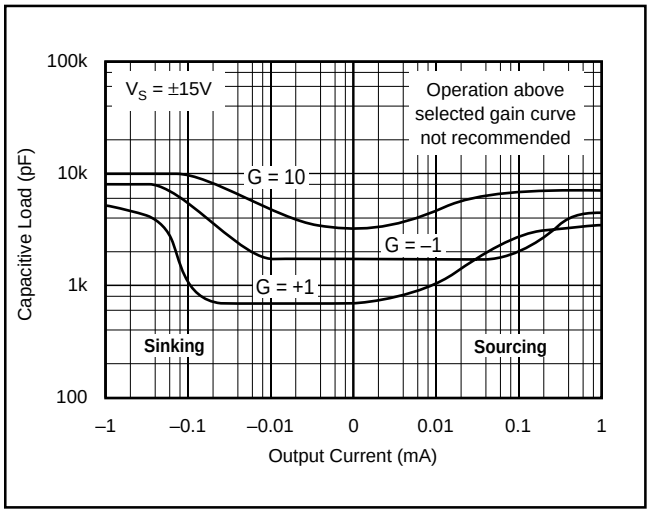


FIGURE 3. Stability—Capacitive Load versus Output Current for ±15V Supplies.

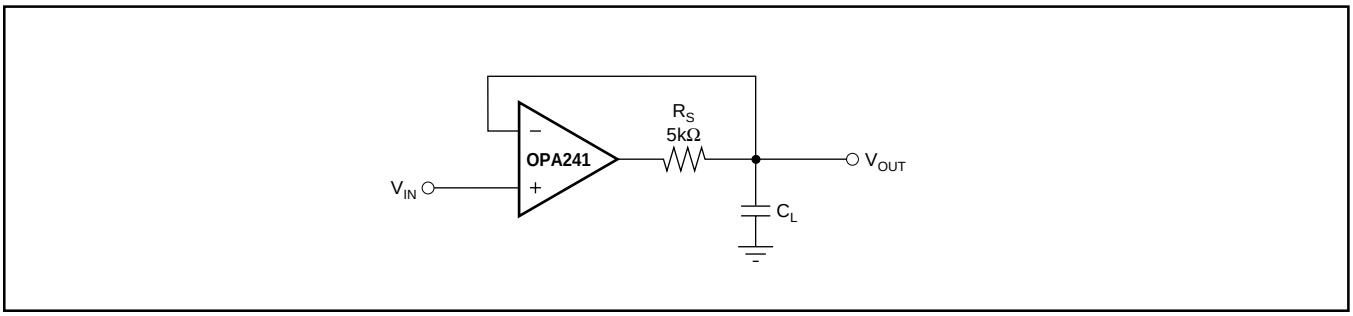
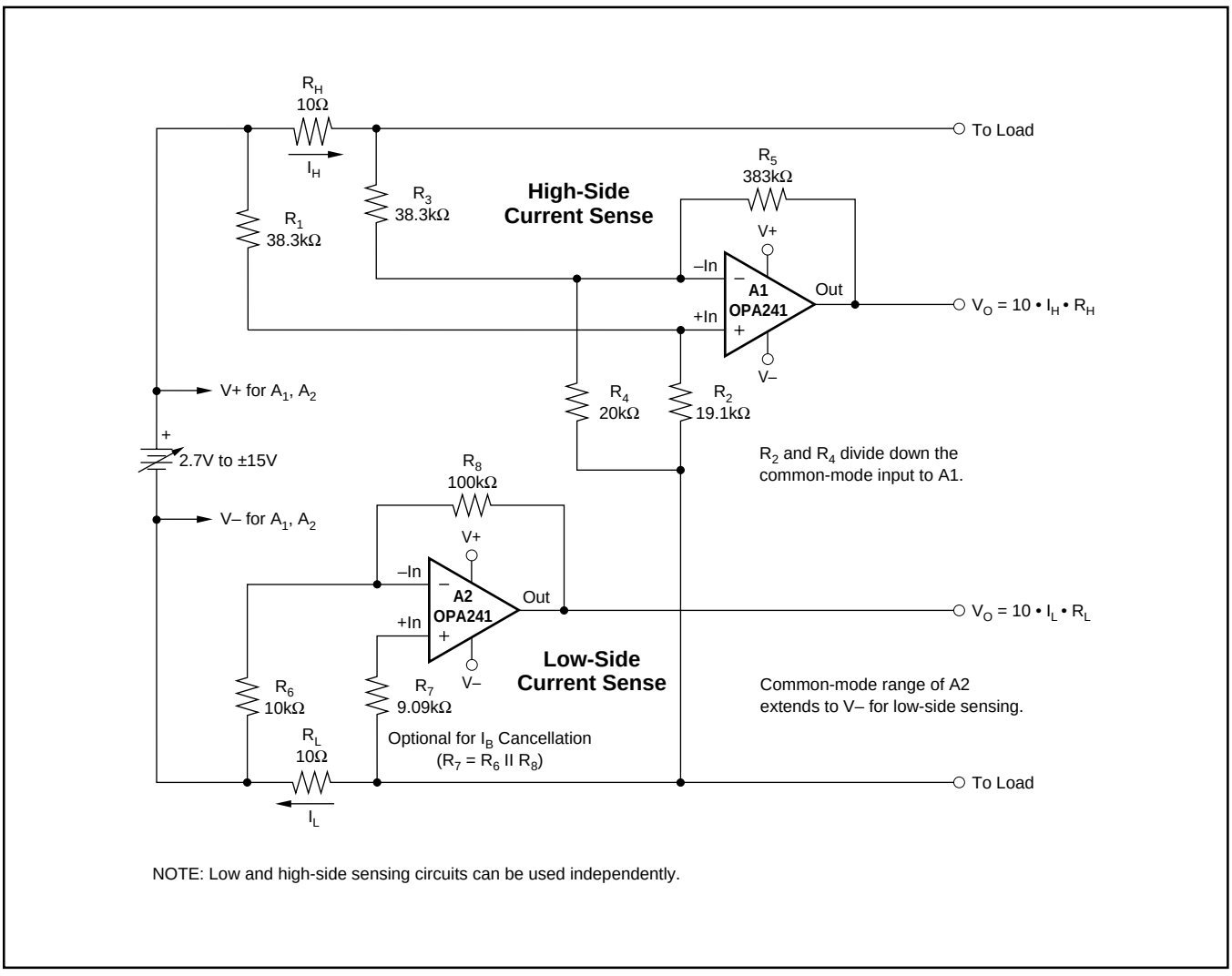


FIGURE 4. Series Resistor in Unity Gain Configuration Improves Capacitive Load Drive.



NOTE: Low and high-side sensing circuits can be used independently.

FIGURE 5. Low and High-Side Battery Current Sensing.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

19-4739; Rev 2; 7/93

MAXIM

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

General Description

The MAX406/MAX407/MAX409/MAX417-MAX419 are single, dual, and quad low-voltage, micropower, precision op amps designed for battery-operated systems. They feature a supply current of less than 1.2µA per amplifier that is relatively constant over the entire supply range, which represents a 15 to 20 times improvement over industry-standard micropower op amps. A unique output stage enables these op amps to operate at ultra-low supply current while maintaining linearity under loaded conditions. In addition, the output is capable of sourcing 1.8mA when powered by a 9V battery.

The common-mode input-voltage range extends from the negative rail to within 1.1V of the positive supply (for the singles, 1.2V for the duals and quads), and the output stage swings rail-to-rail. The entire family is designed to maintain good DC characteristics over the operating temperature range, minimizing the input referred errors.

The MAX406 is a single op amp with two modes of operation: compensated mode and decompensated mode. Floating BW (pin 8) or connecting it to V- internally compensates the amplifier. In this mode, the MAX406 is unity-gain stable with a 5V/ms typical slew rate and an 8kHz gain bandwidth. Connecting BW to V+ puts the MAX406 into decompensated mode with a 20V/ms typical slew rate and a 40kHz gain bandwidth ($A_{VCL} \geq 2V/V$).

The dual MAX407 and quad MAX418 are internally compensated to be unity-gain stable. The MAX409/MAX417/MAX419 single/dual/quad op amps feature 150kHz typical bandwidth, 75V/ms slew rate, and stability for gains of 10V/V or greater.

Applications

Battery-Powered Systems
Medical Instruments
Electrometer Amplifiers
Intrinsically Safe Systems
Photodiode Pre-Amps
pH Meters

Features

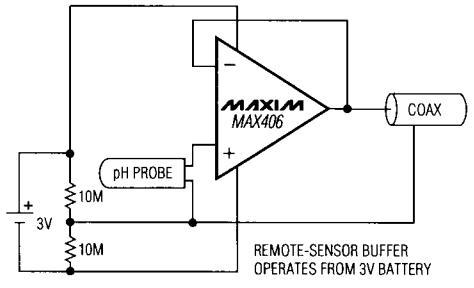
- **1.2µA Max Quiescent Current per Amplifier**
- **+2.5V to +10V Single-Supply Range**
- **500µV Max Offset Voltage (MAX406A/MAX409A)**
- **< 0.1pA Typical Input Bias Current**
- **Output Swings Rail-to-Rail**
- **Input Voltage Range Includes Negative Rail**

Selection Table

PART NUMBER	NO. OF AMPLIFIERS	GAIN-BW PRODUCT (kHz,TYP)	GAIN STABILITY (V/V)	OFFSET VOLTAGE (mV, MAX)
MAX406A	1	8*/40**	1*/2**	0.5
MAX406B	1	8*/40**	1*/2**	2.0
MAX407	2	8	1	3.0
MAX409A	1	150	10	0.5
MAX409B	1	150	10	2.0
MAX417	2	150	10	3.0
MAX418	4	8	1	4.0
MAX419	4	150	10	4.0

** With BW pin open or connected to V-*
*** With BW pin connected to V+*

Typical Operating Circuit



Pin Configurations on last page.

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Continuous Current
All Input Pins 10mA
All Other Pins 50mA
Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
MAX4_ _C_ _ ..... 0°C to +70°C
MAX4_ _E_ _ ..... -40°C to +85°C
MAX4_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Absolute Maximum Ratings do not apply to devices supplied in die or wafer form.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A			0.25	0.5	mV
		MAX406B, MAX409B			0.75	2.0	
		MAX407, MAX417			1.0	3.0	
		MAX418, MAX419			1.0	4.0	
Input Bias Current	I_B	V_{CM} = 0V (Note 2)			<0.1	10.0	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	200	1000		V/mV
			MAX406B, MAX407, MAX409B, MAX41_	100	1000		
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10	23		
Gain Bandwidth	GBW	MAX406A/B	Compensated mode	4	8		kHz
			Decompensated mode (A_V = 2V/V)	20	40		
		MAX407, MAX418		4	8		
		MAX409A/B, MAX417, MAX419, A_{VCL} ≥ 10V/V		80	150		
Input Common-Mode Range	CMR	MAX406A/B, MAX409A/B		V-		V + -1.1	V
		MAX407, MAX41_		V-		V + -1.2	
Output Voltage Swing	V_O	R_L = 1MΩ		±2.47	±2.49		V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	70	80		dB
			MAX406B, MAX407, MAX409B, MAX41_	60	80		
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A		50	100	µV/V
			MAX406B, MAX409B		150	300	
			MAX407, MAX41_		200	600	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Slew Rate	SR	MAX406A/B	Compensated mode	3	5		V/ms
			Decompensated mode (A_V = 2V/V)	12	20		
		MAX407, MAX418		3	5		
		MAX409A/B, MAX417, MAX419 A_{VCL} ≥ 10V/V		40	80		
Supply Current Per Amplifier	I_{SY}				1.0	1.2	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		100	200		µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		300	600		µA
Supply Voltage (V+ to V-)	V_S			2.5		10.0	V
Input Noise Voltage	e_n	f_O = 1kHz			150		nV/√Hz
		f_O = 0.1Hz to 10Hz			6		μV_{p-p}

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				0.95	mV
		MAX406B, MAX409B				3.00	
		MAX407				4.00	
		MAX41_				5.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested			2	10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				20	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	100			V/mV
			MAX406B	50			
		R_L = 1MΩ, (V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407 MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Per Amplifier	I_{SY}				1.6	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	50			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	250			µA

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				1.10	mV
		MAX406B, MAX409B				3.00	
		MAX407, MAX417				4.00	
		MAX418, MAX419				5.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested				10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				50	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	50			V/mV
			MAX406B, MAX407, MAX409B, MAX41_	25			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407, MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	
Supply Current Per Amplifier	I_{SY}					1.7	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		40			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		250			µA

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A, MAX409A				1.5	mV
		MAX406B, MAX409B				4.0	
		MAX407, MAX417				5.0	
		MAX418, MAX419				6.0	
Offset-Voltage Tempco	TC_{VOS}	MAX406A, MAX409A, 100% drift tested				10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				1.0	nA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A, MAX409A	10			V/mV
			MAX406B, MAX407, MAX409B, MAX41_	5			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A, MAX409A	66			dB
			MAX406B, MAX407, MAX409B, MAX41_	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A, MAX409A			150	µV/V
			MAX406B, MAX409B			450	
			MAX407, MAX41_			800	
Supply Current Per Amplifier	I_{SY}					2.0	µA
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		20			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		200			µA

Note 2: Production-automated test equipment cannot resolve input bias currents below 1pA. Lab equipment has shown the MAX40__, MAX41__ typical input bias currents below 0.1pA.

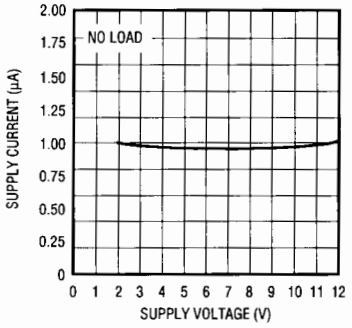
Note 3: MAX406A/MAX409A: V_{CM} = V- to (V+ - 1.1V). MAX407, MAX41_ V_{CM} = V- to (V+ - 1.2V).

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

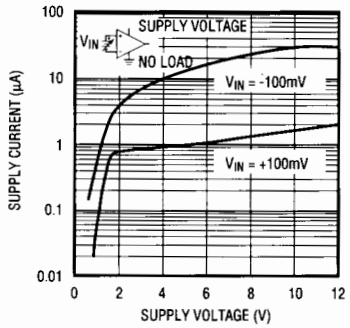
Typical Operating Characteristics

(V+ 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

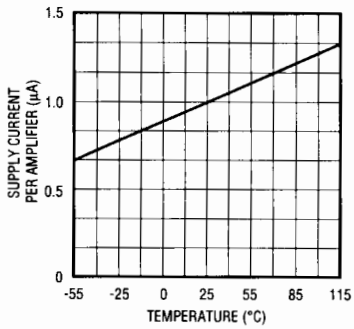
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE



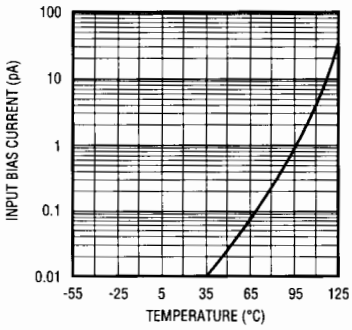
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE IN OVERDRIVE



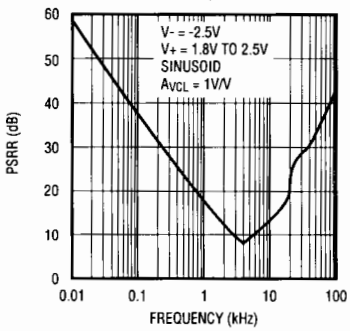
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



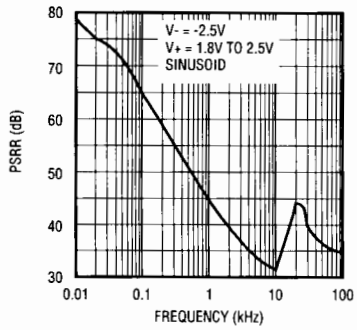
INPUT BIAS CURRENT vs. TEMPERATURE



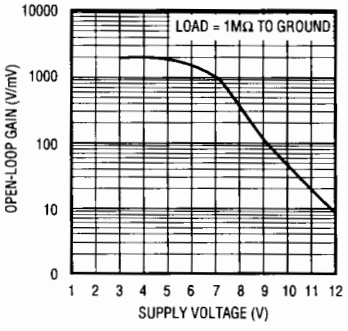
MAX406/MAX407/MAX418 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



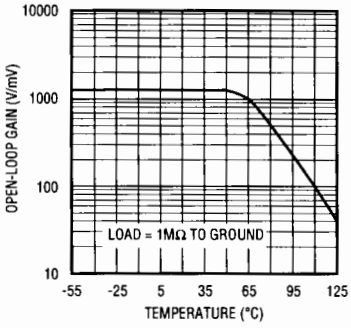
MAX409/MAX417/MAX419 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



LARGE-SIGNAL D.C. GAIN vs. SUPPLY VOLTAGE



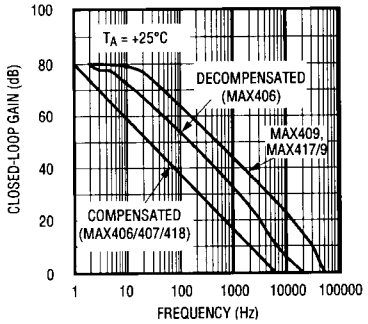
LARGE-SIGNAL D.C. GAIN vs. TEMPERATURE



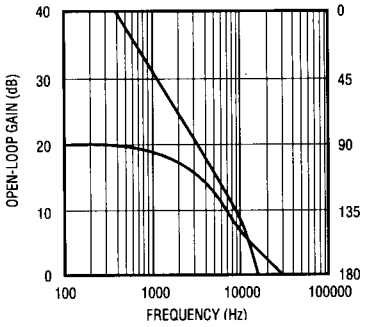
Typical Operating Characteristics (continued)

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted).

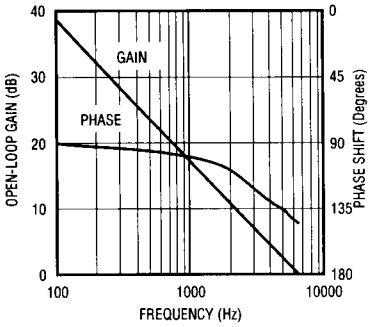
CLOSED-LOOP GAIN (80dB) vs. FREQUENCY



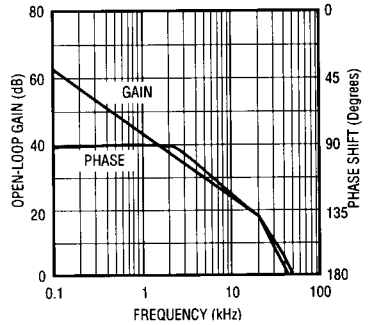
MAX406 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (DECOMPENSATED MODE)



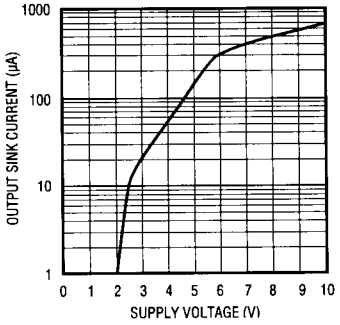
MAX406/MAX407/MAX418 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMPENSATED MODE FOR MAX406)



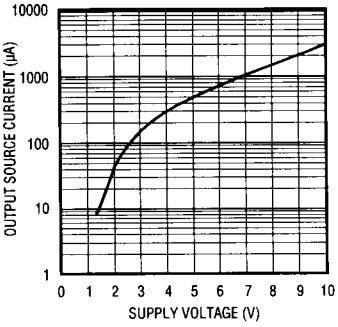
MAX409, MAX417, MAX419 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



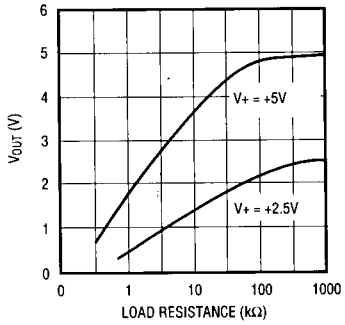
MAXIMUM OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE



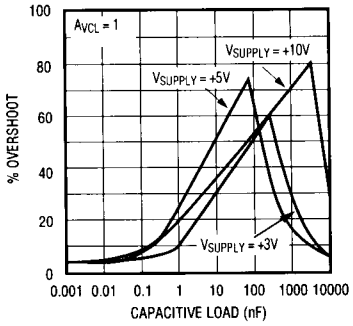
MAXIMUM OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE



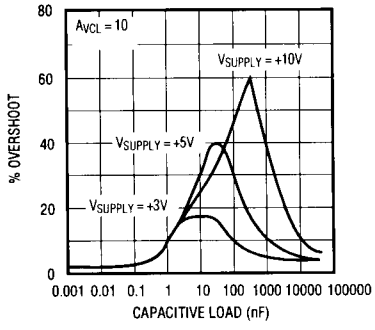
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE (SINGLE SUPPLY)



MAX406, MAX407, MAX418 PERCENT OVERSHOOT vs. CAPACITIVE LOAD (COMPENSATED MODE)



MAX406 PERCENT OVERSHOOT vs. CAPACITIVE LOAD (DECOMPENSATED MODE)

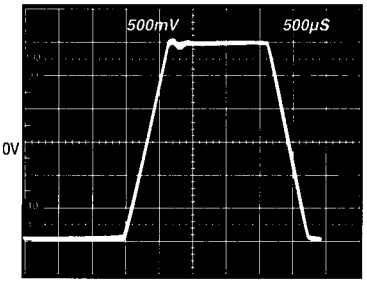


1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

Typical Operating Characteristics

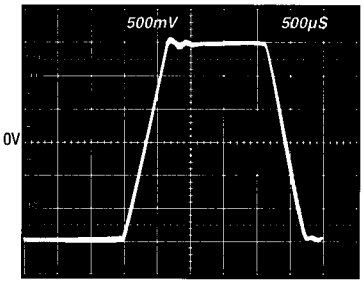
(T_A = +25°C, unless otherwise noted).

MAX406/MAX407/MAX418
LARGE-SIGNAL TRANSIENT RESPONSE



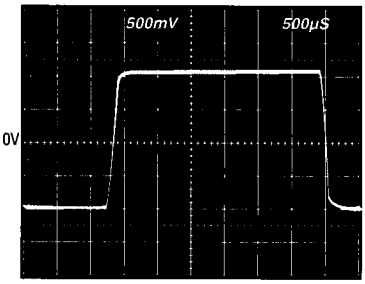
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 250pF

MAX406/MAX407/MAX418
LARGE-SIGNAL TRANSIENT RESPONSE



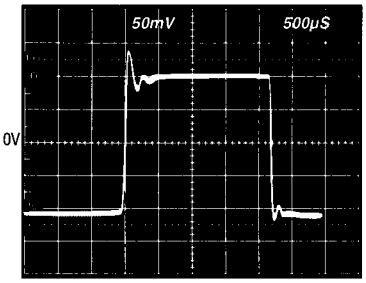
NONINVERTING, A_{VCL} =1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX406 (DECOMPENSATED MODE)
LARGE-SIGNAL TRANSIENT RESPONSE



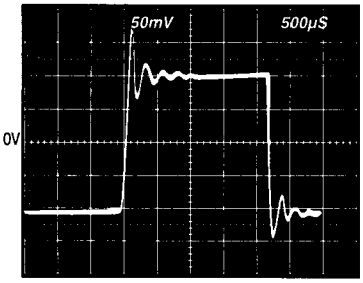
V_{SUPPLY} = ±2.5V, A_{VCL} = 2V/V,
LOAD = 1MΩ II 15pF

MAX406/MAX407/MAX418
SMALL-SIGNAL TRANSIENT RESPONSE



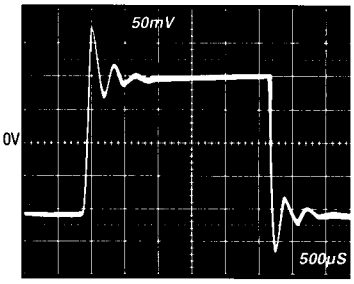
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 250pF

MAX406/MAX407/MAX418
SMALL-SIGNAL TRANSIENT RESPONSE



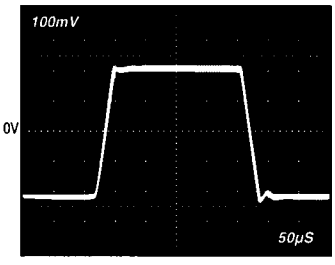
NONINVERTING, A_{VCL} = 1V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX406 (DECOMPENSATED MODE)
SMALL-SIGNAL TRANSIENT RESPONSE



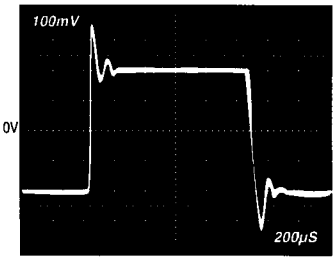
A_{VCL} = 10V/V,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 1000pF

MAX409/MAX417/MAX419
LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 10pF

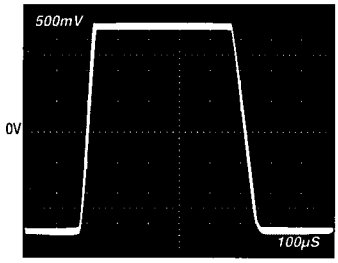
MAX409/MAX417/MAX419
SMALL-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 110pF

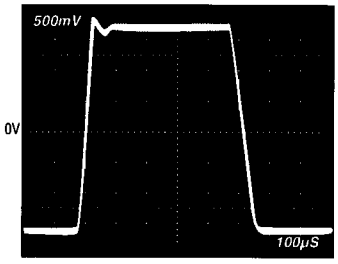
Typical Operating Characteristics (continued)

MAX409/MAX417/MAX419 LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 10pF

MAX409/MAX417/MAX419 LARGE-SIGNAL TRANSIENT RESPONSE



A_V = 10V/V, V_{SUPPLY} = ±2.5V, LOAD = 1MΩ II 110pF

Pin Description

MAX406 PIN	MAX407 MAX417 PIN	MAX409 PIN	MAX418 MAX419 PIN	NAME	FUNCTION
1		1		NULL	Nulling. Connect to one end of 100k potentiometer for offset voltage trimming. See Figure 1.
	1		1	OUTA	Amplifier Output A
2		2		IN-	Inverting Input
	2		2	INA-	Inverting Input A
3		3		IN+	Noninverting Input
	3		3	INA+	Noninverting Input A
4	4	4	11	V-	Negative Power-Supply Pin. Connect to (-) terminal of power supply or ground.
5		5		NULL	Nulling. Connect to one end of 100k potentiometer for offset voltage trimming. Connect wiper to V+. See Figure 1.
	5		5	INB+	Noninverting Input B
6		6		OUT	Amplifier Output
	6		6	INB-	Inverting Input B
7	8	7	4	V+	Positive Supply Pin. Connect to (+) terminal of power supply.
	7		7	OUTB	Amplifier Output B
8				BW	Bandwidth Selection Pin. Leave floating or connect to V- for unity-gain stability (compensated mode) or connect to V+ (decompensated mode).
		8		I.C.	Internal Connection. Make no connection to this pin.
			8	OUTC	Amplifier Output C
			9	INC-	Inverting Input C
			10	INC+	Noninverting Input C
			12	IND+	Noninverting Input D
			13	IND-	Inverting Input D
			14	OUTD	Amplifier Output D

1.2μA Max, Single/Dual/Quad, Single-Supply Op Amps

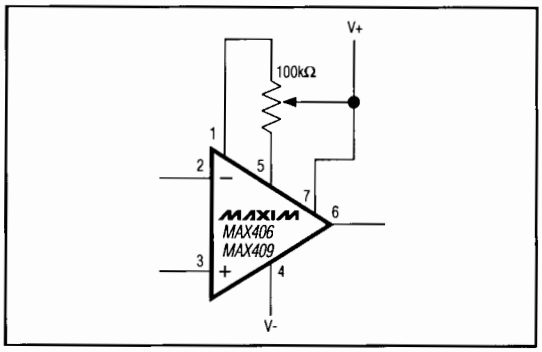


Figure 1. Offset-Voltage Adjustment

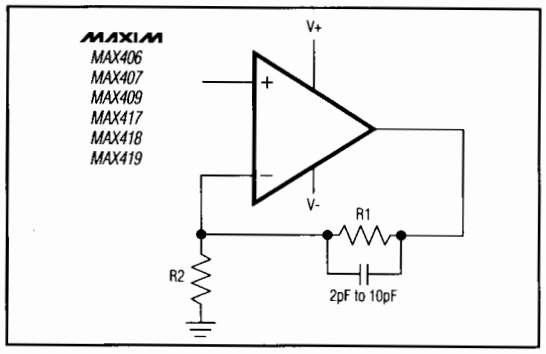


Figure 2. Compensation for Feedback Node Capacitance

Applications Information

Trimming Voltage Offset

The MAX406/MAX409's typical input offset voltage is between 0.25mV and 0.75mV, depending on the grade. If the application requires additional offset adjustment, connect a 100kΩ trim pot between pins 1, 5, and 7 for the MAX406/MAX409 (Figure 1). The dual and quad amplifiers' offset voltages are not adjustable.

Input Overdrive vs. Supply Current

The supply current of the MAX406/MAX407/MAX409/MAX417-MAX419 remains relatively constant over the supply range if the amplifier output is not overdriven to the negative supply rail. For example, when connecting the amplifier as a comparator and applying a -100mV input overdrive, supply current rises above the 1μA per amplifier typical value and varies with supply voltage. (see Supply Current vs. Supply Voltage in Overdrive, *Typical Operating Characteristics*).

Total Supply-Voltage Considerations

Although the MAX406/MAX407/MAX409/MAX417-MAX419 can operate with supply voltages between 2.5V and 10V, best performance is achieved with supply voltages below 7V. The Open-Loop Gain vs. Supply Voltage graph in the *Typical Operating Characteristics* shows how open-loop gain is reduced at voltages that exceed 7V.

Bandwidth

The MAX407/MAX418 are internally compensated for stable unity-gain operation, with an 8kHz typical gain bandwidth. The MAX409/MAX417/MAX419 have a 150kHz typical gain-bandwidth product and are stable with a gain of 10V/V or greater.

The MAX406 operates in one of two modes. Floating BW or connecting BW to V- internally compensates the amplifier for stable unity-gain operation. Connecting BW to V+ reduces the compensation and allows the amplifier to be used at higher speeds. When operating in decompensated mode, the MAX406 is stable for closed loop gains ≥ 2V/V, with a 40kHz typical gain bandwidth and a 20V/ms typical slew rate.

Stability

Unlike other industry-standard micropower CMOS op amps, the MAX406/MAX407/MAX409/MAX417-MAX419 maintain stability in their minimum gain configuration while driving heavy capacitive loads, as demonstrated in the Percent Overshoot vs. Capacitive Load graph in the *Typical Operating Characteristics.*

Although this product family is primarily designed for low-frequency applications, good layout is extremely important. This is because low power requirements demand high-impedance circuits. A 10MΩ impedance and a 1pF capacitance will provide a breakpoint at approximately 16kHz, which is near the amplifier's bandwidth. The layout should minimize stray capacitance at the amplifier's inputs. However, some stray capacitance may be unavoidable, and it may be necessary to add a 2pF to 10pF capacitor across the feedback resistor as shown in Figure 2. Select the smallest capacitor value that insures stability.

Typical Application Circuits

Buffered pH Probe Allows Low-Cost Cable

The MAX406 has less than 20pA input leakage current over the commercial temperature range, and is typically less than 100fA at +25°C. These characteristics are ideal for buffering pH probes and a variety of other high output impedance chemical sensors. The circuit in

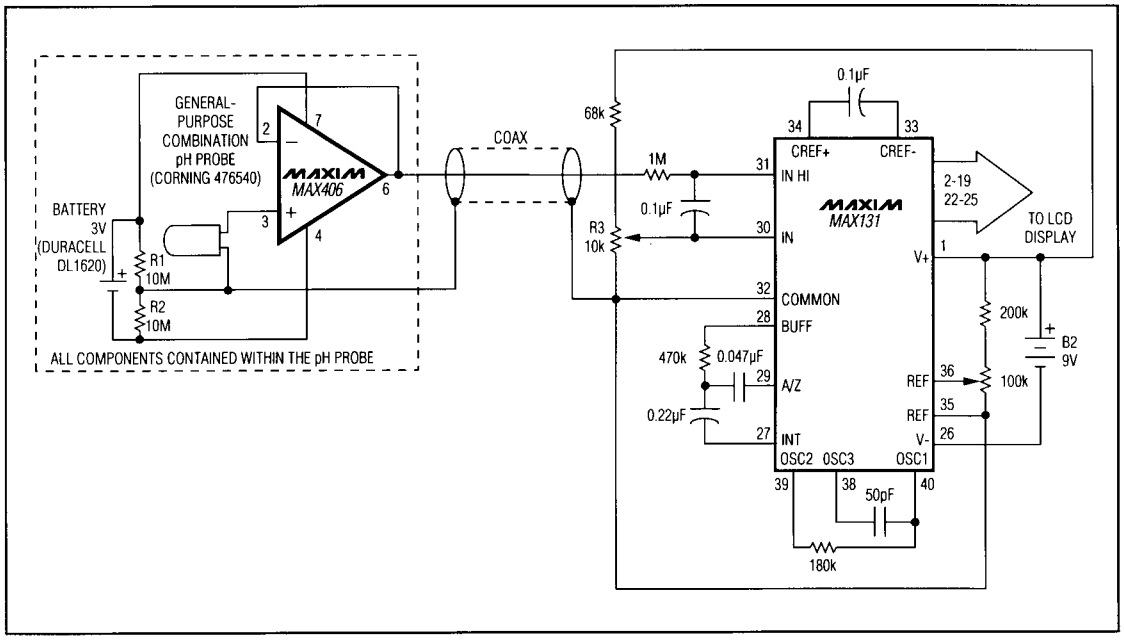


Figure 3. Buffered pH Probe Allows Low-Cost Cable

Figure 3 eliminates expensive low-leakage cables that often connect pH probes to meters. A MAX406 and a lithium battery are included in the probe housing. A conventional low-cost coaxial cable carries the buffered pH signal to the MAX131 A/D converter. In most cases, the probe assembly's battery life exceeds the functional life of the probe itself.

Micropower, 4-Channel Simultaneous Sample-and-Hold

Switch leakage and buffer input bias current in sample and hold circuits limit performance by discharging the signal voltage on the hold capacitor (an effect called "droop"). The 2pA typical room temperature leakage current for the MAX327 and 100fA typical input bias current for the MAX407 translates to a typical droop rate of 200µV/sec for Figure 4's circuit. Another advantage is low power consumption. The MAX327 guarantees no more than 250µA supply current with ±15V supplies, but most of this is drawn by internal logic-level translators. By using rail-to-rail logic (CD4000, 74C00, or 74HC00 families) to drive IN1-IN3, the level translators are turned off and the supply current falls well below 1µA when the switches are off. This technique turns any Maxim switch or multiplexer into an ultra low-power device. Figure 4's circuit typically draws 6µA with 0V to 9V logic input levels.

Remotely Powered Sensor Amp

Figure 5 shows a simple 2-wire current transmitter that uses no power at the transmitting end except from the transmitted signal itself. At the transmitter, a 0V to 1V input drives both a MAX406 and an NPN transistor connected as a voltage-controlled current sink. The 0mA to 2mA output is sent through a twisted pair to the receiver and develops a voltage across the receiver sense resistor R2. The resulting sense voltage is buffered by another MAX406, producing a 0V to 1V ground-referenced output signal. R1 and R2 should be well matched. The MAX406's supply current is added to the 0mA to 2mA signal, resulting in a 500µV offset at the output. This offset, in addition to the MAX406's input offset, varies with temperature.

1.2µA Max, Single/Dual/Quad, Single-Supply Op Amps

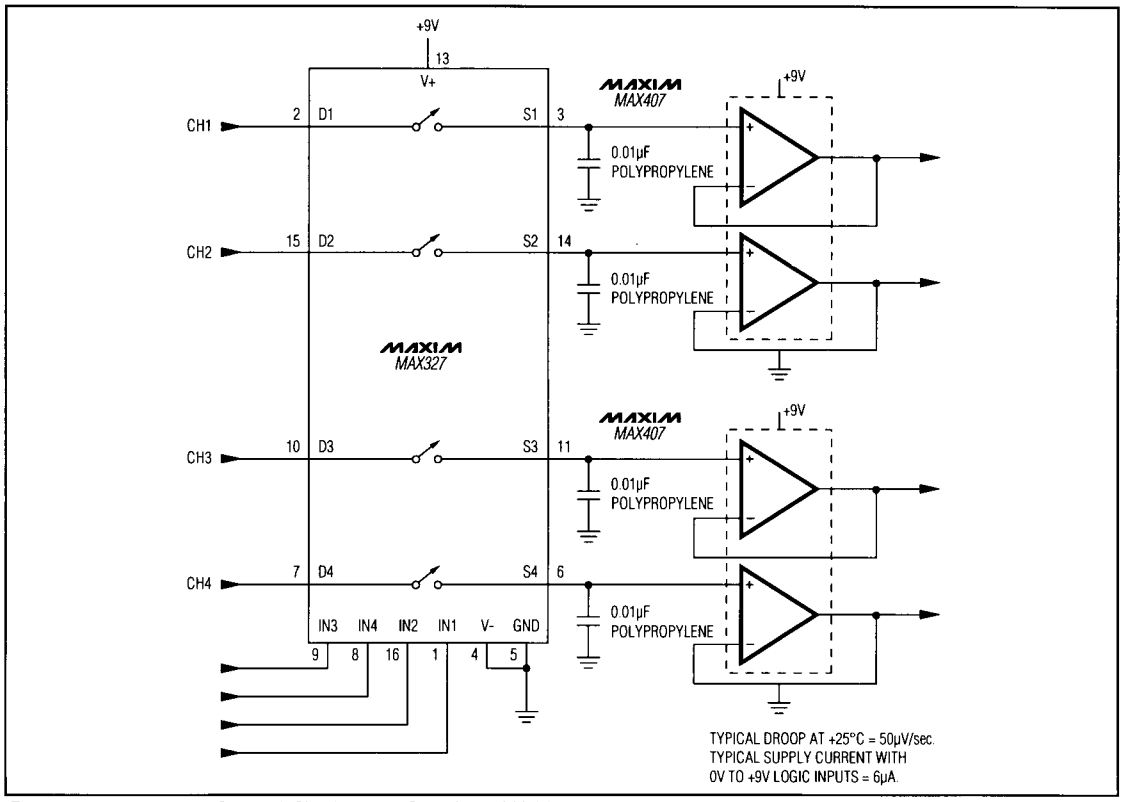


Figure 4. Micropower, 4-Channel, Simultaneous Sample-and-Hold

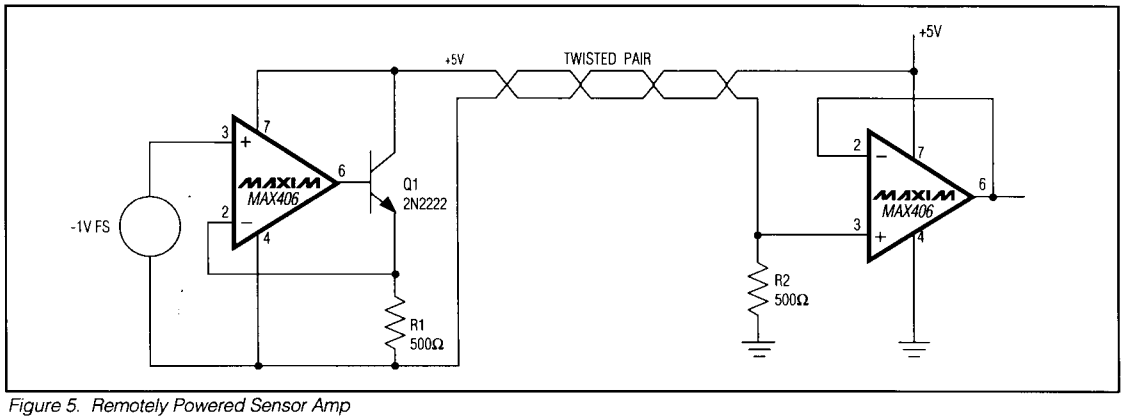


Figure 5. Remotely Powered Sensor Amp

Negative Reference Circuit Draws Less Than 11µA

By biasing a low-power, low-dropout reference (MAX872) so it sits in the feedback path of a MAX406, a precise -2.50V reference is produced that requires no external components, as shown in Figure 6. This is superior to a standard inverting configuration, which requires two resistors that can add errors.

Other advantages of this circuit are:

1. Maximum current drain is 11µA.
2. The output load is driven by the op amp so there is no degradation of voltage due to load regulation.
3. No compensation is needed for load capacitance.

The supplies do not have to be carefully regulated. The positive supply can be as low as 1.1V and the negative supply can be as little as 2.7V.

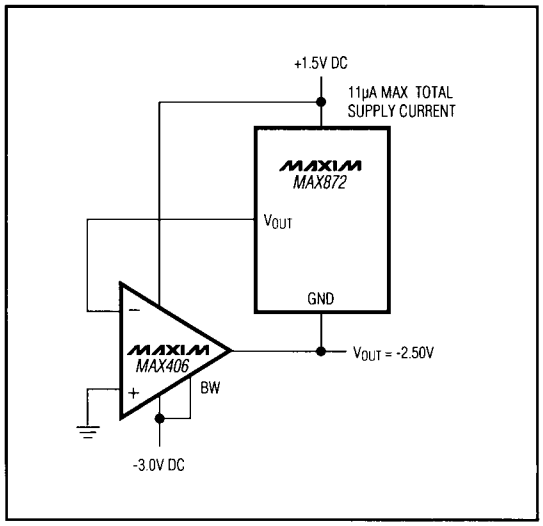


Figure 6. Micropower, Low-Dropout Negative Reference

Ordering Information

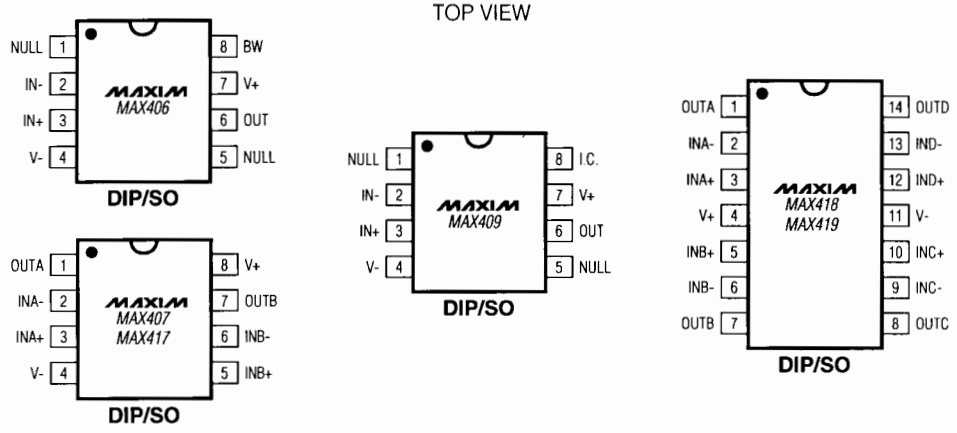
PART	TEMP. RANGE	PIN-PACKAGE
MAX406ACPA	0°C to +70°C	8 Plastic DIP
MAX406BCPA	0°C to +70°C	8 Plastic DIP
MAX406ACSA	0°C to +70°C	8 SO
MAX406BCSA	0°C to +70°C	8 SO
MAX406C/D	0°C to +70°C	Dice*
MAX406AEPA	-40°C to +85°C	8 Plastic DIP
MAX406BEPA	-40°C to +85°C	8 Plastic DIP
MAX406AESA	-40°C to +85°C	8 SO
MAX406BESA	-40°C to +85°C	8 SO
MAX406AMJA	-55°C to +125°C	8 CERDIP
MAX406BMJA	-55°C to +125°C	8 CERDIP
MAX407CPA	0°C to +70°C	8 Plastic DIP
MAX407CSA	0°C to +70°C	8 SO
MAX407C/D	0°C to +70°C	Dice*
MAX407EPA	-40°C to +85°C	8 Plastic DIP
MAX407ESA	-40°C to +85°C	8 SO
MAX407MJA	-55°C to +125°C	8 CERDIP
MAX409ACPA	0°C to +70°C	8 Plastic DIP
MAX409BCPA	0°C to +70°C	8 Plastic DIP
MAX409ACSA	0°C to +70°C	8 SO
MAX409BCSA	0°C to +70°C	8 SO
MAX409BC/D	0°C to +70°C	Dice*
MAX409AEPA	-40°C to +85°C	8 Plastic DIP
MAX409BEPA	-40°C to +85°C	8 Plastic DIP
MAX409AESA	-40°C to +85°C	8 SO
MAX409BESA	-40°C to +85°C	8 SO
MAX409AMJA	-55°C to +125°C	8 CERDIP
MAX409BMJA	-55°C to +125°C	8 CERDIP
MAX417CPA	0°C to +70°C	8 Plastic DIP
MAX417CSA	0°C to +70°C	8 SO
MAX417C/D	0°C to +70°C	Dice*
MAX417EPA	-40°C to +85°C	8 Plastic DIP
MAX417ESA	-40°C to +85°C	8 SO
MAX417MJA	-55°C to +125°C	8 CERDIP
MAX418CPD	0°C to +70°C	14 Plastic DIP
MAX418CSD	0°C to +70°C	14 SO
MAX418EPD	-40°C to +85°C	14 Plastic DIP
MAX418ESD	-40°C to +85°C	14 SO
MAX418MJD	-55°C to +125°C	14 CERDIP
MAX419CPD	0°C to +70°C	14 Plastic DIP
MAX419CSD	0°C to +70°C	14 SO
MAX419EPD	-40°C to +85°C	14 Plastic DIP
MAX419ESD	-40°C to +85°C	14 SO
MAX419MJD	-55°C to +125°C	14 CERDIP

**Dice are specified at +25°C, DC parameters only.*

1.2μA Max, Single/Dual/Quad, Single-Supply Op Amps

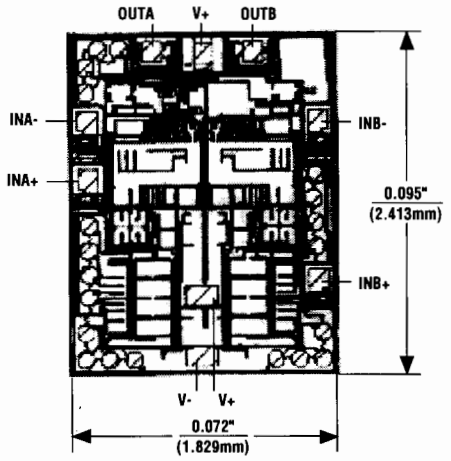
Pin Configurations

TOP VIEW



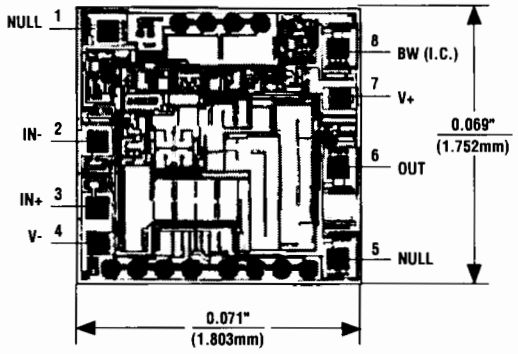
Chip Topographies

MAX407/MAX417



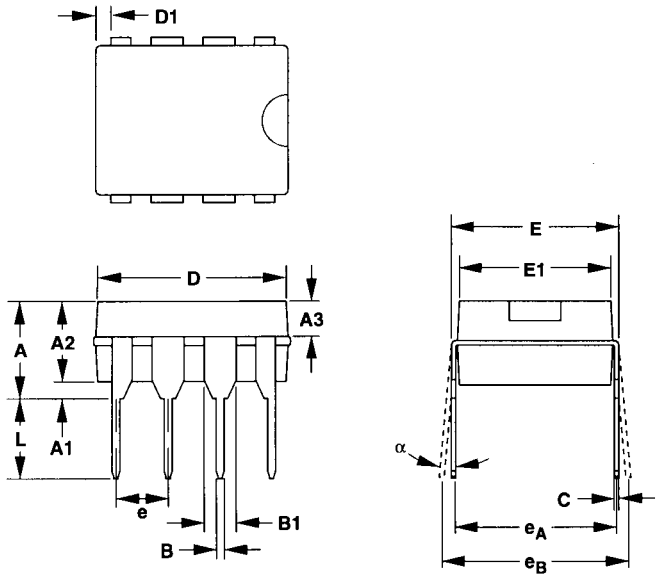
TRANSISTOR COUNT: 98;
SUBSTRATE CONNECTED TO V+.

MAX406/MAX409



TRANSISTOR COUNT: 148;
SUBSTRATE CONNECTED TO V+.

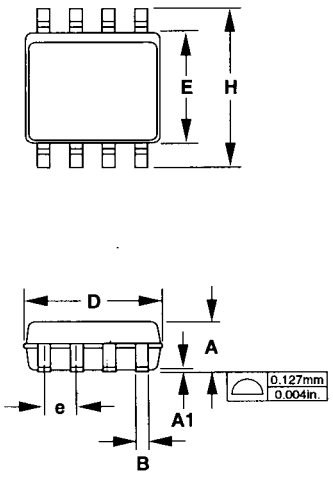
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.348	0.390	8.84	9.91
D1	0.005	0.035	0.13	0.89
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-324A

8-PIN PLASTIC DUAL-IN-LINE PACKAGE



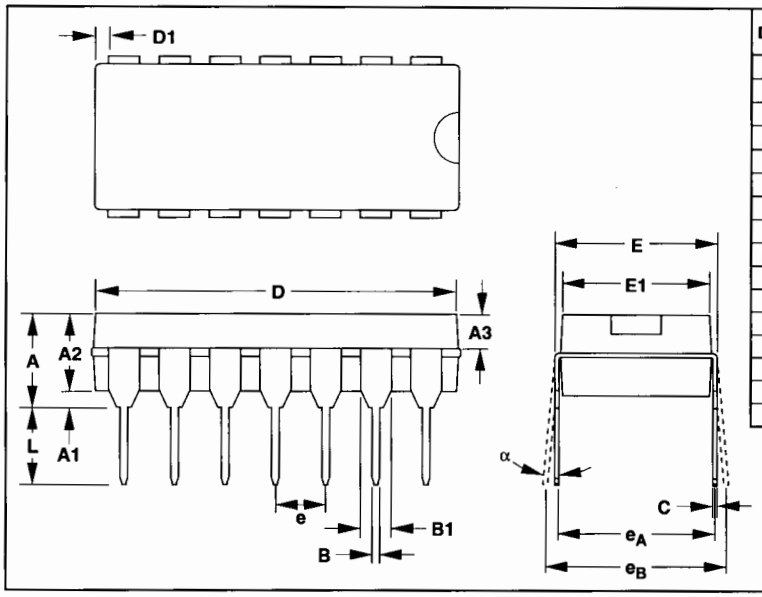
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-325A

8-PIN PLASTIC SMALL-OUTLINE PACKAGE

1.2μA Max, Single/Dual/Quad, Single-Supply Op Amps

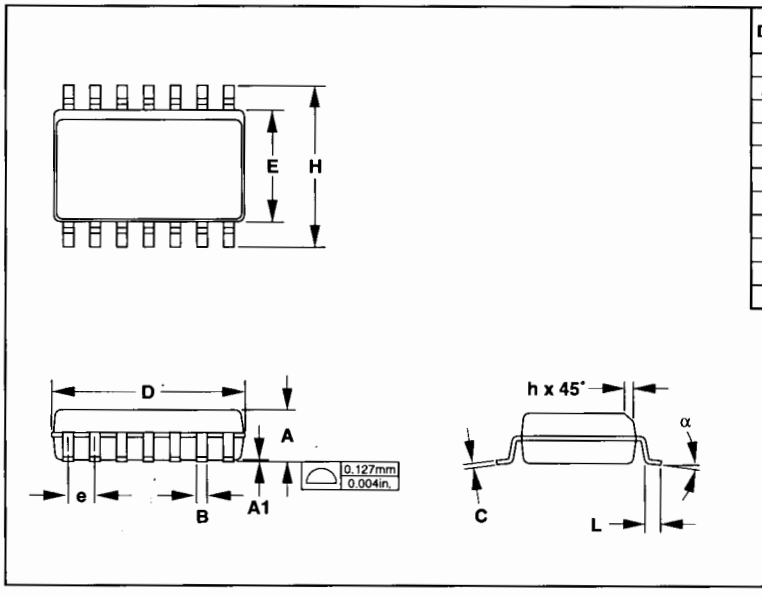
Package Information (continued)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-330A

14-PIN PLASTIC DUAL-IN-LINE PACKAGE



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

21-331A

14-PIN PLASTIC SMALL-OUTLINE PACKAGE