

# ALMA

Atacama Large Millimeter Array

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# **Optical Receiver Board**

David C Brown (dcb@jb.man.ac.uk) Dr Michael Bentley (mikeb@jb.man.ac.uk) JBO - Macclesfield UK JBO - Macclesfield UK



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# **1** OVERVIEW

The optical receiver board accepts three optical inputs modulated at 10Gbits/Sec and converts them to three corresponding NRZI electrical signals for processing by the main receiver board

The main components on the board are the three optical receivers, the Multiplex MTRX192L, which each comprise of a PIN photodiode, a transimpedance amplifier and a limiting amplifier. The gains of these receivers is sufficient to ensure that they can be interfaced directly to following clock and data recovery chips without sacrificing dynamic range.

The performances of the receivers are enhanced by controlling the biasses of the limiting stages by feedback which also serves to compensate for temperature and supply-voltage variations. The power for the receivers is derived from the 48V system bus by well-smoothed, Dc-DC convertors.

The system is controlled and monitored by a PIC 16F877 microcontroller which is interfaced to the ALMA Monitor and Control Bus. The microcontroller measures power-supply voltages through its internal 10-bit analogue-digital converter (ADC), the photocurrents and hence optical power levels into the receivers through Burr-Brown 12-bit ADS7841E ADCs and it controls the compensation circuits through MAXIM 12-bit digital-analogue converters. An RS422 port can signal receiver-power malfunctions back over twisted pairs to the optical amplifiers earlier in the system.

The microcontroller can also turn on and off the DC-DC convertors which power the receivers. The microcontroller and the op-amps in the compensation circuits are powered directly fom the 5 and 12 volt supplies from the mainboard. The status of the system can be monitored and controlled via the AMCB.

# **2** INTERFACES

- 1 The Main Receiver Board. Reference 1 and Section 3.3.1.2.
- 2 ALMA Monitor and Control Bus. References 2 and 3.
- 3 Optical Switch. Reference not available.
- 4 Optical Amplifier Control System. Reference not available..

# **3** SPECIFICATIONS

# 3.1 Performance Specifications

# 3.1.1 General

The module will convert optical signals to electrical signals with a bit error rate of less than 1 in 10<sup>10</sup> when the inputs levels are within the specification of section 3.1.2.

### 3.1.2 Inputs

For correct operation the optical inputs will be in the range 0dBm to -20dBm. If the inputs are outside the range +2 dBm to - 23dBm the module will signal a fault to the optical amplifier control system.

# 3.1.3 Outputs

Electrical outputs are single ended AC coupled signals with an impedance of 50 ohms and a minimum level of 500 mV p-p

# 3.2 Monitor and Control Interface

# 3.2.1 General

The board is connected to the ALMA M&C interface by an SPI bus to an AMBSI module on the main board. The protocol and timing of the SPI bus are described in reference 2.

The interface will be configured to work with a fixed size monitor data length of eight bytes within an address space of 256 bytes. In practice less than 80 points are meaningful and of these only 32 may be written to. Prior to receiving an ID request the interface will work in mode 0 (chip select deasserted after every byte). After sending the ID it will work in mode 1 ( chip select deasserted only at the end of the transfer.

# 3.1.5 Summary of Monitor and Control Points

_STATUS1	0x20	Primary status		
STATUS2	0x20	Secondary status		
_OPOVAL_M	0x22		MS 4 bits	
OPOVAL L	0x23	Current value - Optical Rx 0	LS 8 bits	
OP1VAL M	0x24	Ourseland on the De t	MS 4 bits	
OP1VAL_L	0x25	Current value - Optical Rx 1	LS 8 bits	
OP2VAL M	0x26	Currentuckus Ontical Du 0	MS 4 bits	
OP2VAL L	0x27	Current value - Optical Rx 2	LS 8 bits	
_0120742_1	0/12/			
_VNVAL_M	0x28	Current value - Negative PSU	MS 2 bits	
_VNVAL_L	0x29		LS 8 bits	
_VPVAL_M	0x2A	Current value - Positive PSU	MS 2 bits	
_VPVAL_L	0x2B		LS 8 bits	
_TMPVAL _M	0x2C	Current value - Temperature	MS 2 bits	
_TMPVAL_L	0x2D		LS 8 bits	
_VCVAL_M	0x2E	Current value - Control PSU	MS 2 bits	
_VCVAL_L	0x2F		LS 8 bits	
	0x30	Not used		
	0x31			
_OP0FLT_M	0x32	Fault value - Optical Rx 0	MS 4 bits	
_OP0FLT_L	0x33		LS 8 bits	
_OP1FLT_M	0x34	Fault value - Optical Rx 1	MS 4 bits	
_OP1FLT_L	0x35		LS 8 bits	
_OP2FLT_M	0x36	Fault value - Optical Rx 2	MS 4 bits	
_OP2FLT_L	0x37		LS 8 bits	
_VNFLT_M	0X38	Fault value - Negative PSU	MS 2 bits	
_VNFLT_L	0x39	5	LS 8 bits	
_VPFLT_M	0x3A	Fault value - Positive PSU	MS 2 bits	
_VPFLT_L	0x3B		LS 8 bits	
_TMPFLT_M	0x3C	Fault value - Temperature	MS 2 bits	
_TMPFLT_L	0x3D	•	LS 8 bits	
_VCFLT_M	0x3E	Fault value - Control PSU	MS 2 bits	
_VCFLT_L	0x3F		LS 8 bits	
COMMAND	0x40	Command Pagister		
	0x40 0x41	Command Register Not used		
OP1ULIM_M	0x41 0x42	Upper limit - Optical Rx 0		#
	0x42 0x43	Lower Limit - Optical Rx 0		#
	0x43 0x44	Upper limit - Optical Rx 0		#
OP1LLIM L	0x44 0x45	Lower Limit - Optical Rx 1		#
OP1LLIM_L	0x45 0x46	Upper limit - Optical Rx 1		#
	0x40 0x47	Lower Limit - Optical Rx 2		#
	0847			#

VNULIM	0x48	Upper limit - Negative PSU		#
VNLLIM	0x49	Lower limit - Negative PSU		#
VPULIM	0x48	Upper limit - Positive PSU		#
VPLLIM	0x4B	Lower limit - Positive SU		#
	0x4D 0x4C	Upper limit - Temperature		#
	0x4C 0x4D	Lower limit - Temperature		#
VCULIM	0x4D 0x4E	-		#
—		Upper limit - Control PSU Lower limit - Control PSU		
_VCLLIM	0x4F	Lower limit - Control PSU		#
ODOFT M	0.50	_		
_OP0FT_M	0x50	Fine Tune - Optical Rx 0	MS 4 bits	#
_OP0FT_L	0x51		LS 8 bits	#
_OP1FT_M	0x52	Fine Tune - Optical Rx 1	MS 4 bits	#
_OP1FT_L	0x53		LS 8 bits	#
_OP2FT_M	0x54	Fine Tune - Optical Rx 2	MS 4 bits	#
_OP2FT_L	0x55		LS 8 bits	#
_OP0CAL1_M	0x56	0dB cal - Optical Rx 0	MS 4 bits	#
_OP0CAL1_L	0x57		LS 8 bits	#
_OP0CAL0	0x58	Zero cal - Optical Rx 0		#
_OP1CAL1_M	0x59	0dB cal - Optical Rx 1	MS 4 bits	#
_OP1CAL1_L	0x5A		LS 8 bits	#
_OP1CAL0	0x5B	Zero cal - Optical Rx 1		#
_OP2CAL1_M	0x5C	0dB cal - Optical Rx 2	MS 4 bits	#
_OP2CAL1_L	0x5D		LS 8 bits	#
_OP2CAL0	0x5E	Zero cal - Optical Rx 2		#
_	0x5F	Not used		#
_ID0	0x64	Identity Request Bytes	1	
_ID1	0x65		2	
ID2	0x66		3	
CHECK	0x67	Checksum of EPROM		
_SN_M	0x60	Board Serial Number	MS 8 Bits	
 SN_L	0x61		LS 8 Bits	
 VN_M	0x62		MS 8 Bits	
 VN_L	0X63	Program version number	LS 8 Bits	
_CRC_M	0x64		MS 8 Bits	
_CRC_L	0x65	CRC16 of program code	LS 8 Bits	
	0,100			

# indicates locations that can be written to. Attempts to write to other locations will be ignored without notification

# 3.1.6 Summary of Commands

Ready for command	0x00	
Resend the fine tune parameters	0x01	
Calibrate Rx0 at zero input	0x02	
Calibrate Rx1 at zero input	0x03	
Calibrate Rx2 at zero input	0x04	
Calibrate Rx0 at 1mW input	0x05	
Calibrate Rx1 at 1mW input	0x06	
Calibrate Rx2 at 1mW input	0x07	
Reload parameters from EEPROM	0x08	
Save parameters in EEPROM	0x09	
CalibratingRx0 at zero input	0x0A	#
Calibrating Rx1 at zero input	0x0B	#
Calibrating Rx2 at zero input	0x0C	#
Calibrating Rx0 at 1mW input	0x0D	#
Calibrating Rx1 at 1mW input	0x0E	#
Calibrating Rx2 at 1mW input	0x0F	#
Turn PSUs off	0x10	
Turn PSUs on	0x11	
Assert EDFA shutdown line	0x12	
Deassert EDFA shutdown line	0x13	
Blank the LED display	0x14	
Enable the LED display	0X15	
Regenerate CRC	0X16	
Command has failed	>0x7F	#

# These commands should not be sent. When a calibration command has been accepted the command register is increased in value by eight. If the calibration is completed successfully the command register is returned to zero. Otherwise it is set to a value greater than 0x7F and the calibration factor is not updated. Sending any command not in this table will return 0xFF.

# 3.1.7 Monitor Points in Detail

### 3.1.7.1 General

There are, in principle, 256 function points corresponding to the first 256 RAM locations in the PIC. In practice only 74 are defined and only 32 of these can be written to.

#### 3.1.7.2 Actual Measurements.

These are monitored by the PIC several times a second and urgent action is taken if they go out of specification. It should be possible for maintenance engineers to call up these values on demand. It would also be desirable for the control computer to log these values occasionally so that long term trends can be monitored in an attempt to anticipate failures. These values are read-only to the control computer. Attempts to write to them will be ignored without warning.

#### 3.1.7.2.1 -2 volt power supply for receivers

This is a ten bit number occupying two bytes. The resolution is 5mV; the range is 2.555 to 0 volts Formally: V = (N-512)/200 where N is the nine bit reading

 $10111ahy. V = (1V 312)/200 \text{ where Wisther have being the time bit in the bit is the time bit in the bit in the bit is the time bit is the b$ 

### 3.1.7.2.2 3.3 volt power supply for receivers

This is a ten bit number occupying two bytes. The resolution is 5mV; the range is 0 to 5.115 volts Formally: V = N/200 where N is the ten bit reading

#### 3.1.7.2.3 8 volt auxiliary power supply

This is a ten bit number occupying two bytes. The resolution is 10mV; the range is 0-10.23 volts

Formally: V = N/100 where N is the ten bit reading

#### 3.1.7.2.4 The temperature

This is a ten bit number stored in a two bytes. The resolution is 0.25°C; the range is -60°C to 195°C.

Formally: T = N/4 - 60 where N is the ten bit reading.

- 3.1.7.2.5 The optical power for receiver 0
- 3.1.7.2.6 The optical power for receiver 1

#### 3.1.7.2.7 The optical power for receiver 2

These are twelve bit numbers occupying two bytes. The resolution is 0.5uW; the range is 0 to 2.0475mW. However these are nominal figures and each receiver must be calibrated at two points. n0 is the reading with no input; n1 the reading with 1mW input.

Formally: P = (N-n0)/(n1-n0) mW where N is the twelve bit reading

The reading should also be available in decibels: reference level 1mW = 0dBm.

#### 3.1.7.2.8 Invalid Data

It is possible that an SPI interrupt could occur whilst the PIC is updating a reading. If this happened the two bytes of the data might belong to different samples. The PIC will flag this situation by setting the MS bit of the MS byte whilst the reading is going on.

If this bit is set in any reading the data should be disregarded. As an update takes 1uS and occurs every 10mS the possibility of a clash, with its associated software overhead, is very low.

### 3.1.7.3 Safety Limits

These are the limits against which the measurements in section 1 are compared by the PIC. Should any reading go out of limits the PIC will take immediate action before informing the control computer. These limits are stored in the EEPROM and are loaded into data RAM at start up. They can be read and written by the M&C bus. When new limits are sent they are only loaded into the data RAM. To save them in EEPROM requires a command.

- 3.1.7.3.1 -2v power supply lower and upper limits. (1.8 to 2.2 volts)
- 3.1.7.3.2 **3.3v power supply lower and upper limits** (3.0 to 3.6 volts)
- 3.1.7.3.3 8v power supply lower and upper limits. (7.0 to 9.0 volts)
- **3.1.7.3.4** Temperature lower and upper limit (-60°C to 70°C)

Each limit is stored as a single byte which must be multiplied by four to obtain the actual value. The resolution is reduced but is still adequate. The lower limit for temperature is included only for consistency with the voltage measurements and will be set to -60°C.

- 3.1.7.3.5 Optical power lower and upper limits for receiver 0 (See section 3.1.2)
- 3.1.7.3.6 Optical power lower and upper limits for receiver 1 (See section 3.1.2)
- **3.1.7.3.7** Optical power lower and upper limits for receiver 2 (See section 3.1.2)

The upper limit is a four bit number stored in a single bytes which must be multiplied by 256 to obtain the actual value. The lower limit is an eight bit number stored in a single byte, the upper four bits always being zero.

## 3.1.7.4 Parameters For Optical Receivers.

These parameters are stored in the EEPROM and are loaded into data RAM at start up. They can be read and written by the control computer. When new parameters are sent they are only loaded into the data RAM. To save them in EEPROM will require a command.

## 3.1.7.4.1 Calibration

The calibration parameter n0 is an eight bit number stored in a single byte, the upper four bits always being zero. The calibration parameter n1 is a twelve bit number stored in two bytes in the same format as the measurement.

These calibration parameters can be read by the control computer to allow it to compute the actual power levels. For convenience they will be able to be written. However meaningful calibration can only be achieved by running a correct calibration procedure. This would normally be done in the laboratory under local control. For completeness the same calibration commands could be included in the control computer.

### 3.1.7.4.2 Fine Tuning

Each receiver needs a fine tuning voltage which is derived from a twelve bit DAC. Each fine tuning parameter is a twelve bit number stored in two bytes. Altering these parameters is a two stage process. First the RAM locations must be updated. Then a command must be issued to reload the DACs.

### 3.1.7.5 Fault Reports.

When a fault occurs and a power supply or optical amplifier shut down is commanded the PIC will save the values of the appropriate measurements . The control computer should be able to deduce the reason for the shutdown from these readings. Similarly when a reset occurs (which may or may not be a fault) the reason for the reset is saved.

### 3.1.7.5.1 Primary status word.

- Bit 7 The optical fault line is asserted
- Bit 6. The main power supplies are shut down
- Bit 5 The serial number of the board could not be obtained at start-up.
- Bit 4 Check sum fail when reading EEPROM
- Bits 3..0 The reason for the last restart

0001	MCLR/ Reset
0010	Power On Reset
0011	Brown Out Reset
0100	Watch Dog Time Out Reset

### 3.1.7.5.2 Secondary status word

If bit 6 of the primary word is set then bits 3..0 of the secondary word are the reason for the PSU shutdown

0000	None	PSUs have not been started
0001	Over temperature	
0010	8 volt fault	During startup
0011	8v fault + overtemp	
0100	-2volt fault	
0101	+3.3volt fault	
0110	+8volt fault	After PSUs have started
0111	Over temperature	
1000	M&C command	

If bit 7 of the primary word is set then bits 7..4 of the secondary word are the reason for the EDFA shutdown command being sent

0000	No measurements taken yet
0001	Receiver 0 Fault
0010	Receiver 1 Fault
0011	Receiver 2 Fault
0100	+8volt PSU Fault
0101	M&C command
0110	SPI timeout

#### 3.1.7.5.3 3.3v power supply value before shutdown

- 3.1.7.5.4 2v power supply value before shutdown
- 3.1.7.5.5 8v power supply value before shutdown.
- 3.1.7.5.6 Temperature before shutdown

These are meaningful only if bit 7 of the master status word is set. They have the same format as the corresponding measurements.

#### 3.1.7.5.7 Optical power before shutdown - receiver 0

3.1.7.5.8 Optical power before shutdown - receiver 1

#### 3.1.7.5.9 Optical power before shutdown - receiver 2

These are only meaningful if bit 6 of the master status word is set. They have the same format as the corresponding measurements.

#### 3.1.7.6 Miscellaneous

#### 3.1.7.6.1 Board Serial Number and Revision Level.

This is a 16 bit number occupying two bytes. The upper four bits are the revision level, the lower twelve the serial number. It is unique for every board and cannot be changed. If bit 5 of the primary status word is set this number is not meaningful and the serial number is unknown.

#### 3.1.7.6.2 Software Revision Level

This is a 16 bit number occupying two bytes. It can only be changed by reprogramming the PIC

### 3.1.7.6.3 ID Request Bytes

These are three bytes as defined in Reference 2.

#### 3.1.7.6.4 Checksum

When parameters are stored in the EEPROM a simple checksum is generated and stored. When the parameters are read back the checksum is recomputed. If it is incorrect a bit is set in the primary status word and the fault syndrome is stored at the checksum location.

#### 3.1.7.6.5 CRC

The CRC of the entire program code is computed at start up and stored. This can be read and compared with a published correct value. Additionally, if it is suspected that the code is corrupt the PIC can be commanded to regenerate the CRC for comparison with earlier versions.

The CRC is generated across the first 2048 words of code, which have been initially erased to 0x3FFF. Each 14 bit word is zero extended to 16 bits The generator polynomial is

 $x^{16} + x^{12} + x^{5} + 1$ , the CRC being initialized to 0xFFFF.

# 3.1.8 Commands in Detail

### 3.1.8.1 General

To execute a command it is necessary to write the command code to the command register (monitor point 0x40). When the command has been successfully executed the micro-controller will return the command register to zero. If the command fails the micro-controller will put a negative number in the register. During execution of a command the contents of the register may change but will always be a positive non zero number

### 3.1.8.2 EEPROM commands

#### 3.1.8.2.1 Update EEPROM from RAM

#### 3.1.8.2.2 Reload RAM from EEPROM

When modifications are made to the parameters or limits they are only written to the RAM and will be lost at restart unless they are saved in EEPROM. If mistakes are made in modifying the parameters the original values can be recovered from EEPROM. A checksum is generated and stored when data is written to the EPROM. The checksum is recomputed on reading from the EPROM and if a fault is detected the appropriate bit in the primary status word is set.

#### 3.1.8.3 Power Supply

#### 3.1.8.3.1 Shut down power supplies

3.1.8.3.2 Restart power supplies.

Starting the powers supplies takes approximately 100mS. The shut down time is not defined

### 3.1.8.4 Optical fault Line

3.1.8.4.1 Activate Optical Fault line

#### 3.1.8.4.2 Deactivate Optical Fault line

These commands are provided for test purposes only

#### 3.1.8.5 Calibration

- 3.1.8.5.1 Calibrate Rx 0 at zero input.
- 3.1.8.5.2 Calibrate Rx 1 at zero input.
- 3.1.8.5.3 Calibrate Rx 2 at zero input.
- 3.1.8.5.4 Calibrate Rx 0 at 1mW input.
- 3.1.8.5.5 Calibrate Rx 1 at 1mW input.
- 3.1.8.5.6 Calibrate Rx 2 at 1mW input.

The correct optical level must be on the appropriate input before issuing these commands. After accepting the command the micro-controller increases the command code by eight to show that the command is in progress. It then makes 256 measurements at 10mS intervals and computes the average.

If the average is reasonable it is written to the appropriate RAM and the command register set to zero. If the value is unreasonably low the command register is set to -2 or if it is too high it is set to -1.

These commands take approximately 2.5 seconds to execute.

#### 3.1.8.6 Fine Tuning Parameters

This command resends the fine tuning parameters to the DAC in the control loop

#### 3.1.8.7 CRC

This causes the CRC of the code to be regenerated.

#### 3.1.8.8 LED Display

#### 3.1.8.8.1 Enable the LEDs

#### 3.1.8.8.2 Blank the LEDs

The LED displays are a useful diagnostic aid but at other times they are an unnecessary power drain. They will be enabled at initialization.

# **3.2 Physical Specifications**

# 3.2.1 Packaging

### 3.2.1.1 General

The receiver module is assembled on a printed circuit board sized  $102mm \times 221mm$  with six layers (four buried power planes and two surface tracked. It is mounted as a mezzanine 15mm above the main receiver board. The receiver modules are in 12 pin butterfly packages with an SMA connector for the digital output on one edge and a fiber flying lead for the optical input from the facing edge. The modules are mounted through cut-outs in the edge of the board. All three modules are screwed to a common aluminum plate of size  $175mm \times 51mm$  which is attached to the circuit board by 5mm spacers. This plate both acts as a heat sink and provides mechanical support.

The two through-hole DC-DC converters are mounted on the underside of the board and occupy space between the mezzanine and main boards. The remaining components, which are a mixture of surface and through-hole mounting, are mounted on top of the board.

A cover plate of transparent material is mounted 15mm above the mezzanine and extends the full length of the main board. This provides attachment points and protection against snagging for the optical fiber inputs.

### 3.2.1.2 Connectors

#### 3.2.1.2.1 Power and control

Power and control lines are brought onto the board through a 40-pin PC104 connector, the male part of which is mounted on this board.

1	48V LINE	2	48V RET	21	MCLR/	22	GND
3	48V LINE	4	48V RET	23	EDFA-A	24	GND
5	-	6	GND	25	CS/	26	GND
7	12V	8	GND	27	CLK	28	GND
9	12V	10	GND	29	SDI	30	GND
11	-	12	GND	31	SDO	32	GND
13	5V	14	GND	33	5V OUT	34	GND
15	-	16	GND	35	PGM	36	GND
17	-	18	GND	37	PGC	38	GND
19	EDFA-B	20	GND	39	PGD	40	GND

### 3.2.1.2.2 Optical

The three optical fiber flying lead inputs terminate in Diamond E-2308.6 blind mate connectors on the backplane connector of the main board.

#### 3.2.1.2.3 R.F. Electrical

The 10GHz electrical outputs are connected to the main board by RG402 (Belden 1673A) cable terminated in SMA plugs.

#### 3.2.1.3 Front panel

The front panel is shared with the main receiver board. Piercings will be required for eight 5mm LEDs.

### 3.2.2 Power Dissipation and Thermal Interface

The power dissipation of each receiver module is approximately 750 mW. The dissipation of the rest of the components is less than 200mW. Assuming power supply efficiency is 75% the total dissipation is about 3.2Watts.

The power supplies are built with 50mm x 25mm aluminum heat sinks. The three receiver modules are mounted on a common 175mm x 51mm x 2mm aluminum plate.

The power dissipation of this board should be taken into account when designing the thermal interface for the main board.

# 3.2.3 Weight

Approximately 350gms (12.5oz).

# **4 FUNCTIONAL DESCRIPTION**

See figure 1 for the block diagram and figures 2-5 for the full circuit diagram

# 4.1 General

The module can be described as three functional units: power supplies, optical receivers and their immediate support circuitry and the micro-controller and its associated monitor and control circuitry.

### 4.1.1 **Power Supplies**

The receiver modules require power supplies of +3.3 volts at 110mA and -2.0 volts at 160mA, approximately 2 Watts in all. These supplies are derived from the main 48-volt bus using Texas Instruments PT4220 series DC-DC converters. The outputs of these converters are extensively filtered as the receiver module is very sensitive to switching noise on its power supplies. These two power supplies can be switched on and off by the supervisory micro-controller through opto-isolators.

A clean eight volt supply is required to bias the PIN diodes and to power some of the control circuitry. This is supplied by a linear regulator, type MC78L08 taking its input from the main board 12-volt line. Finally the supervisory micro-controller and associated digital components require a 5-volt supply. This is taken directly from the main board.

All supplies are fused and filtered where they enter the board and are protected against voltage transients.

# 4.1.2 Optical Receivers

These are type MTRX192L manufactured by Multiplex Inc. These modules contain:

- a reverse biased PIN diode, which converts the optical signal to an analog electrical signal.
- a trans-impedance amplifier which amplifies this signal.
- a limiting amplifier which acts as a single-bit A-D converter.

The limiting amplifier is essentially a comparator whose threshold level can be set externally. The receiver module generates a monitor output by integrating the main output. An external feedback loop adjusts this threshold level so as to maintain the monitor output at the value which gives the best signal-to-noise ratio. The circuit used is substantially that recommended by the manufacturer (Appendix D).

This value must be determined experimentally and is set by the supervisory micro-controller which communicates it to the feedback loop via a D-A converter, type MAX525. For optimum performance, additional compensation for operating temperature and supply voltage are incorporated into the feedback loop.

The bias current in the PIN diode is a direct representation of the optical input power and is determined by measuring the voltage drop across a 1K5 series resistor. The supervisory micro-controller can read this value through an A-D converter. The anticipated range of optical input levels is +3 to -30dBm (2mW to 1uW). Satisfactory resolution over this range requires a 12 bit analog to digital converter, Analog Devices type ADS7841.

Although the relationship between received power and bias current is linear, the slope and zero offset can vary slightly between individual receiver modules. Each device must be calibrated and the calibration numbers stored in the supervisory micro-controller

The ADCs and DACs share a 2.56-volt reference which is derived from a type LM4051 adjustable voltage reference diode.

## 4.1.3 Supervisory micro-controller

### 4.1.3.1 General

This is a PIC16F877 (Reference 4) clocked at 20MHz. The key features of this chip are:

- 8K words of program memory
- 368 bytes of data memory
- 256 bytes of non-volatile data memory
- SPI serial communications interface
- 8 input 10-bit analog to digital converter (reduced to 2 inputs when using SPI interface)
- 21 further digital I/Os
- In-circuit low voltage programming

The micro-controller performs these monitoring and control tasks:

- Setting the levels for the limiting amplifier feedback loops.
- Monitoring the optical power levels
- Monitoring the temperature
- Monitoring the power supplies
- Switching the power supplies

The ambient temperature near the heat-sink and the values of the three voltage rails generated on the board are monitored using the 10-bit ADC internal to the supervisory micro-controller, fed by an analog multiplexer, type MC14052.

The micro-controller is responsible for the integrity of the receiver modules and the safety of the link:

- If the temperature or voltages are not within prescribed limits, the receiver module power supplies will be switched off.
- If an optical power level is too high (representing possible damage to the PIN diode) or too low (indicating a possible break in a fiber) a shutdown signal is sent to the appropriate optical amplifier.
- If the eight-volt power supply fails, confidence in the measurements is lost. The receiver module power supplies are turned off and the optical shutdown signal is sent.

The micro-controller communicates with upstream optical components over a dedicated RS422 serial link driven by a MAX487 transceiver. This provides a quicker and more secure method of shutting down the optical link if it is suspected that a hazardous situation, such as a broken fiber, exists. The protocol for this link has not yet been defined. At its simplest it need be no more than a single go/no signal. The polarity is arranged so that a break in the link will be interpreted as a fault signal

Each board has a unique 16-bit identification number (4-bit revision level and 12-bit serial number). This is stored in a PIC12C508 (Reference 4) and transferred over a single line on request. A six pin header permits in-circuit programming and debugging.

The safe limits for power supplies and temperature, the calibration factors, the threshold levels and other parameters are stored in non volatile memory. This memory can be accessed by the M&C system.

## 4.1.3.2 Micro-controller Configuration

#### 4.1.3.2.1 Ten bit analog inputs

The +3.3 and -2.0 powers lines to the modules, the +8volt reference level and the temperature near the optical modules are measured using a single channel of the internal ADC and a 4 way analog multiplexer. Two digital outputs are used to operate the multiplexer. A second input, with another multiplexer is available for expansion.

(A quirk in the PIC design means that only two of the eight analog inputs can be used when the SPI bus is configured to use the chip select pin)

#### 4.1.3.2.2 Higher Resolution Analog Inputs

The optical power of each of the three optical modules is measured. The resolution needed for these is greater than ten bits so an external twelve bit converter is used. This is a quad device with an SSI serial connection. An SSI connection, independent of that to the M&C bus, is implemented in software.

#### 4.1.3.2.3 DACs for Fine Tuning of Optical Modules

Three DACs are required and these can be obtained in a single package with an SSI serial connection,. This SSI bus is the same one used for the ADCs, the only extra pin being another chip select.

#### 4.1.3.2.4 Serial Link to AMBSI-II Module

This uses the standard SSI bus, in slave mode, implemented in the PIC hardware. In addition the chip select line is connected to the PIC external interrupt pin. Use of the interrupt pin simplifies servicing SPI requests.

### 4.1.3.2.5 In Circuit Serial Programming And Debugging

In circuit serial programming requires three dedicated pins which are also used by the microchip in-circuit debugger. These pins are not available for use on the board.

#### 4.1.3.2.6 Power Supplies Switching

This requires two outputs, one for the +3.3v and one for the -2.0v. These are connected to the power supplies by opto-isolators in such a way that that it is necessary for the PIC to sink current to turn on the supplies. As the pins are initially configured as inputs at start up the power supplies will be off.

#### 4.1.3.2.7 EDFA shutdown

This requires a single output which enables an RS422 driver.

#### 4.1.3.2.8 LEDs

Up to eight diagnostic LEDs can be fitted, though only two are currently allocated - power supply shutdown and EDFA shutdown. Port D is reserved for these LEDs.

### 4.1.3.2.9 Identification PIC

This requires two lines. A request output (which resets the identification PIC) and a data input over which the number is transferred using pulse width coding. The program code for this PIC is given in appendix 2.

# 4.1.3.2.10 Summary of Pin Use

		Usage	Туре	PLCC
RA0	AN0	Analog inputs	а	3
RA1	AN1	Spare analog inputs	а	4
RA2				5
RA3	Vref+	A-D reference	а	6
RA4				7
RA5	CS/	External-SSI chip select	i	8
RB0	INT	External SSI chip select	i	36
RB1	RB1	+3.3v switch	0	37
RB2	RB2	-2.0v switch	0	38
RB3	PGM	ICSP select	x	39
RB4	RB4	EDFA switch	0	41
RB5	RB5	Serial number request	0	42
RB6	PGC	ICSP clock	X	43
RB7	PGD	ICSP data	x	44
RC0	RC0	Local SSI clock	0	16
RC1	RC1	Local SSI data in	i	18
RC2	RC2	Local SSI data out	0	19
RC3	SCLK	External SSI clock	i	20
RC4	SDI	External SSI data in	i	25
RC5	SDO	External SSI data out	0	26
RC6	RC6	Internal SSI ADC chip select	0	27
RC7	RC7	Internal SSI DAC chip select	0	29
RD0	RD0	EDFA LED	0	21
RD1	RD1	Power LED	0	21
RD2	RD2	Diagnostic LED	0	23
RD3	RD2	Diagnostic LED	0	23
RD4	RD4	Diagnostic LED	0	30
RD5	RD5	Diagnostic LED	0	31
RD6	RD6	Diagnostic LED	0	32
RD7	RD7	Diagnostic LED	0	33
RE0	RE0	Analog multiplexer sel0	0	9
RE1	RE1	Analog multiplexer select 1	0	10
RE2	RE2	Serial number in	i	11

i digital input pino digital output pina analog input pinx special function pin

## 4.1.3.3 Micro-controller Software

A detailed software listing is available in appendix A.

#### 4.1.3.3.1 Initialisation

At reset the board will be in safe mode. Prior to attempting to establish contact with the AMBSI the micro-controller will execute the following initialization tasks:

- Configure the inputs and outputs.
- Establish and save the reason for the reset..
- Obtain the serial number of the board and the software revision level
- Copy parameters and limits from EEPROM to RAM.
- Calculate a cyclic redundancy code for the first 2048 program words.

The micro-controller then waits until it receives a Null Transfer (ten consecutive zeros) before continuing with these start up tasks.

- Enable interrupts all subsequent SPI transfers are dealt with under interrupt.
- Send the DC voltage to each receiver control loop.
- Measure the temperature.
- Measure the control voltage.

If the control voltage is within limits the dedicated optical control line is set to no fault. If the temperature is also satisfactory the power supplies are turned on. The micro-controller then enters the main loop.

### 4.1.3.3.2 Main Loop

This executes in about 10mS and performs the following tasks:

- Measure the positive and negative voltages and the temperature If any of these are out of spec the power fault routine is called
- Measure each of the optical power levels If any of these are out of spec the optical fault routine is called
- Measure the control voltage If this is out of spec both fault routines are called
- Check that that an SPI transfer has been received within the last 2.5 seconds If not, the optical fault routine is called.
- Check whether a command has been written to the command register If so, execute it.

### 4.1.3.3.3 Fault Actions

The PSU fault routine first ascertains whether the power supplies have already been shut down. If so no further action is taken. Otherwise the latest readings of voltage and temperature are stored in the appropriate registers. The status word is set to indicate the nature of the fault that precipitated the shutdown.

The optical fault routine first ascertains whether an optical fault is already signaled. If so no further action is taken. Otherwise the latest readings of the optical levels are stored in the appropriate registers. The status word is set to indicate which receiver precipitated the shutdown.

It should be noted that special status codes are used to indicate that no attempt has yet been made to turn on the power supplies or clear the optical fault line. And to indicate that a fault was detected during start up.

# 5 SETUP AND MAINTENANCE

# 5.1 Setup

The setup procedure given below is the cautious one used on the locally assembled prototypes. It is anticipated that a simpler procedure will be used on production boards.

# 5.1.1 Initial checks

The board should be initially assembled without the optical receiver modules being mounted. A 100K resistor should be temporarily connected between pins 1 and 2 at each module position.

It should than be connected to an M&C bus or an M&C bus emulator and the following tests performed:

- Check, with a digital voltmeter, that the control voltage at Q100:1 is  $8.0v \pm 0.1v$ .
- Check, with a digital voltmeter, that the reference voltage at Q200:2 is  $2.56v \pm .05v$ .
- Using the M&C bus, check that the temperature reading is reasonable and that it changes when the temperature sensor Q201is heated or cooled.
- Using the M&C bus check that the optical power level for each receiver is -10dBm  $\pm$  0.5dBm.

Remove the resistors and temporarily short pins 7 & 8 at each module position

• Using the M&C bus adjust the fine tuning parameter (for all three modules) and measure the voltage shown (x=3,4,5):

Fine tune parameter = 0%	Voltage on Cx16 = $0.40 \pm .05$	Voltage on Ux00:7 = $-1.50 \pm .1$
Fine tune parameter = 100%	Voltage on Cx16 = $0.89 \pm .05$	Voltage on Ux00:7 = $-1.00 \pm .1$
Fine tune parameter = 50%	Voltage on Cx16 = $0.63 \pm .05$	Voltage on Ux00:7 = -1.27 $\pm$ .1

Leave the fine tuning parameters set to 50% and remove the shorts.

# 5.1.2 Safety limits

Check the safety limits against those given in section 3.1.7.3 and correct them if necessary.

# 5.1.3 Optical Modules

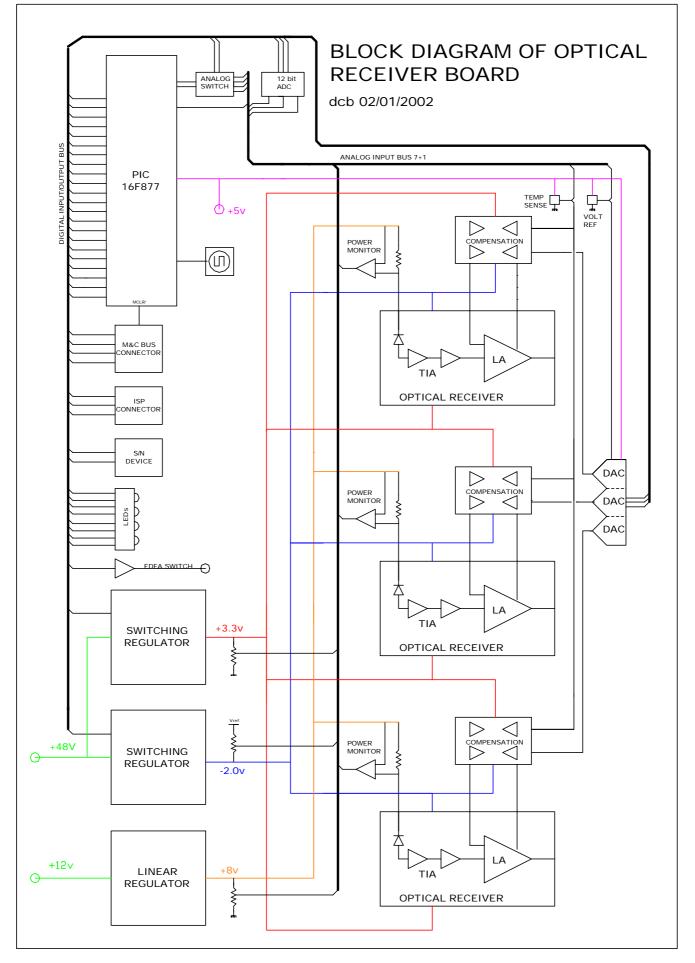
The optical modules may now be mounted, using the jig shown in figure 8 and the heat sink fitted as shown in the same figure.

Each module should then be calibrated at zero input and at 0dBm (1mW) by applying the correct input level and issuing the appropriate calibration command (section 3.1.8.5). If an accurate input source is not available the manufacturer's calibration figures should be used. If this is not available set the calibration factors to their defaults of 0000 and 2048.

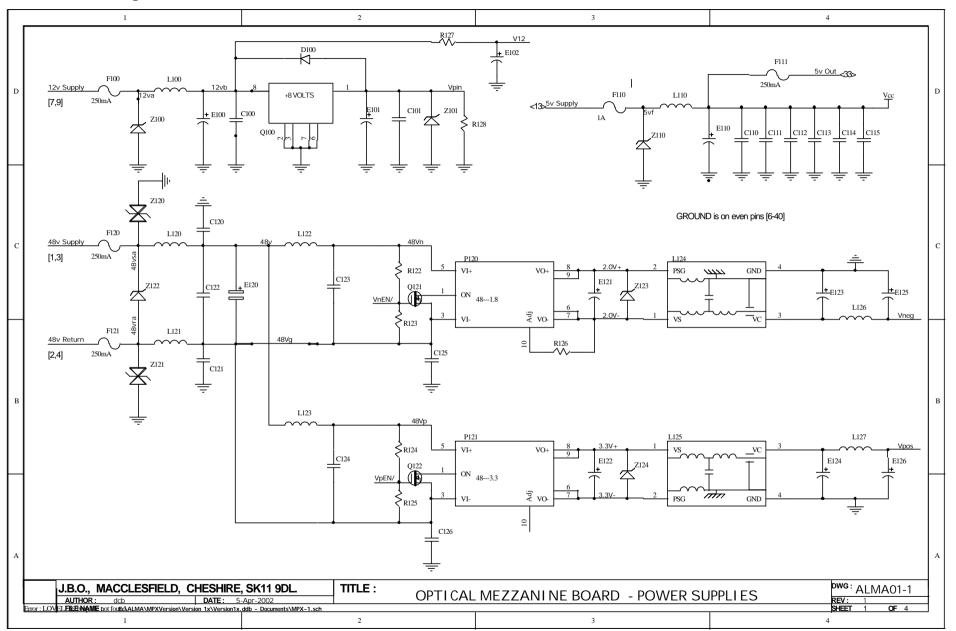
Proper operation of the module when connected to a light source modulated with a pseudo random pulse sequence at 10Gb/s should be confirmed. Photo 3 shows the eye diagrams obtained on the prototype.

# 6 **REFERENCES**

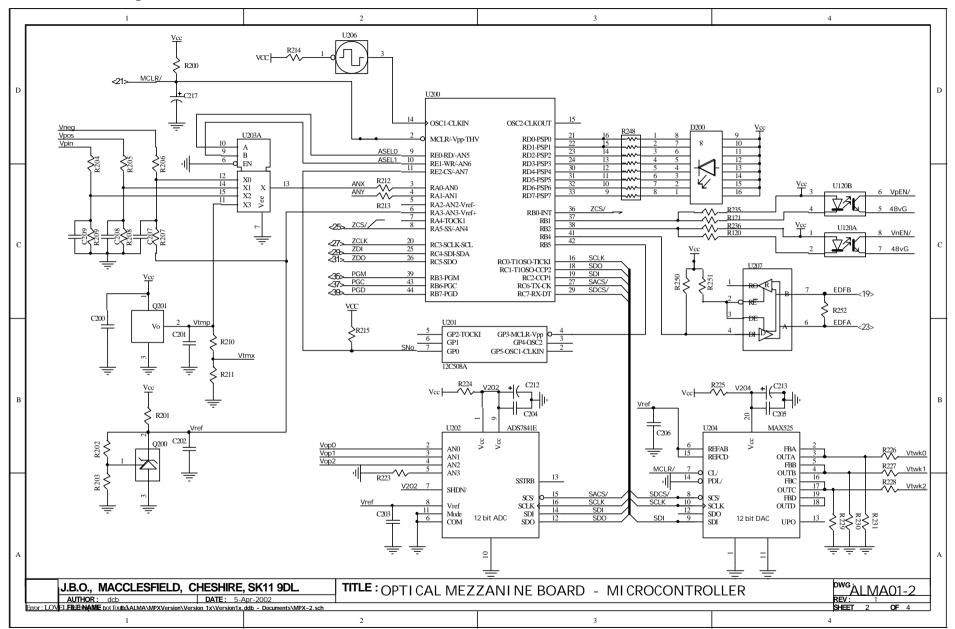
- 1 Hardware specification of main receiver board
- 2 AMBSI Standard Interface: ALMA-SW-0012 Wayne Kowski. 2001-05-02
- 3 ALMA Monitor and Control Bus Interface Specification ALMA--SW-007 Mick Brooks, Larry D'Addario. 2001-02--05
- 4 PIC16F877 data sheets . PIC 12C508A data sheets Arizona Microchiphttp://www.microchip.com



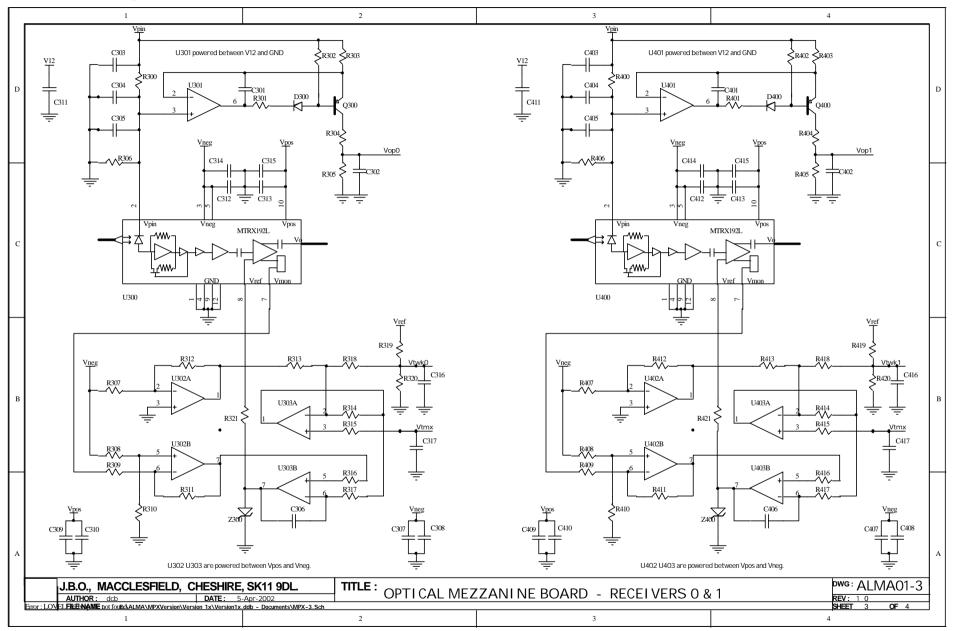
# 7.1.2 Circuit Diagram 1



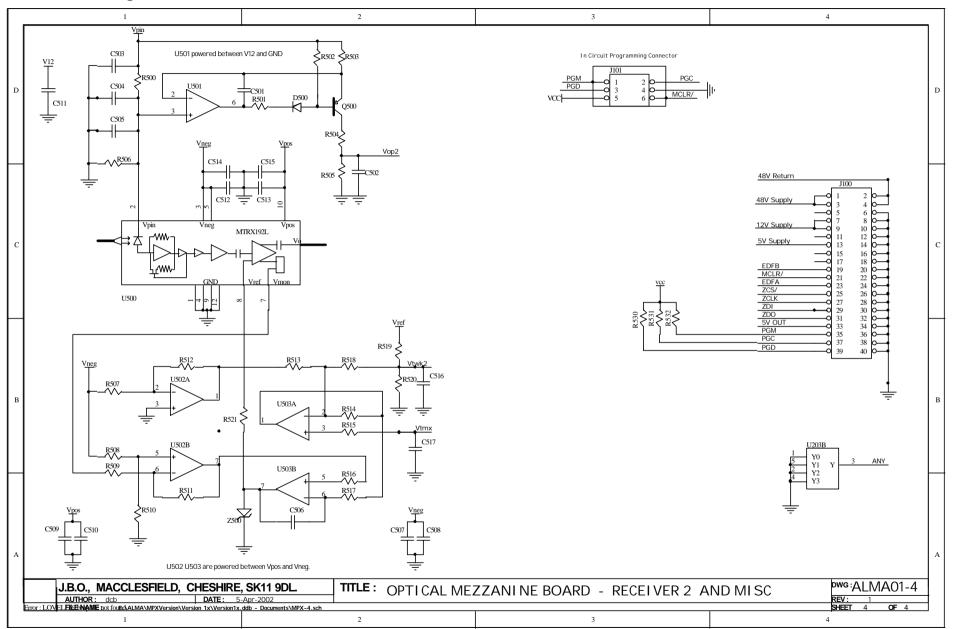
# 7.1.3 Circuit Diagram 2

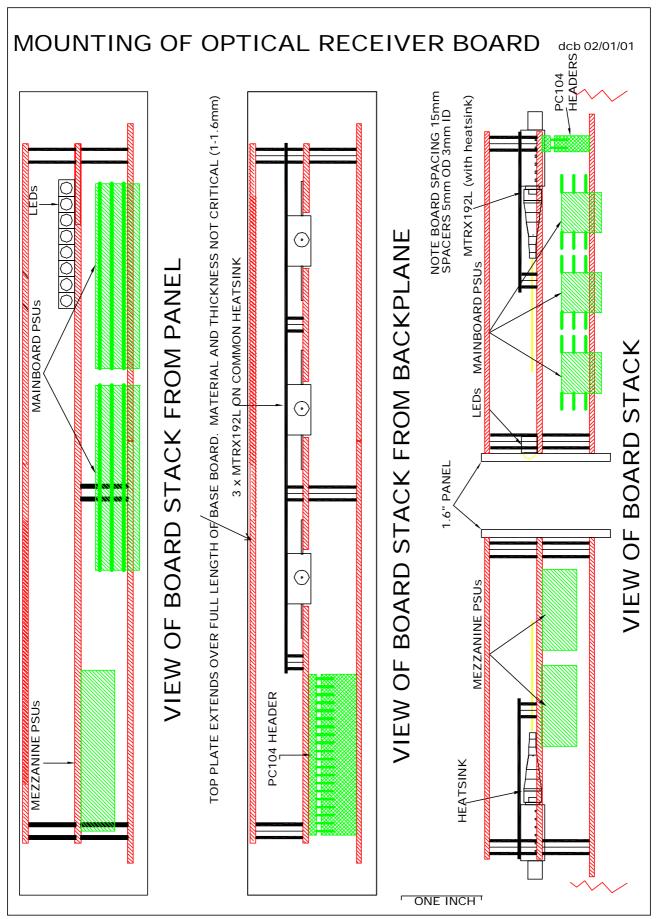


# 7.1.4 Circuit Diagram 3

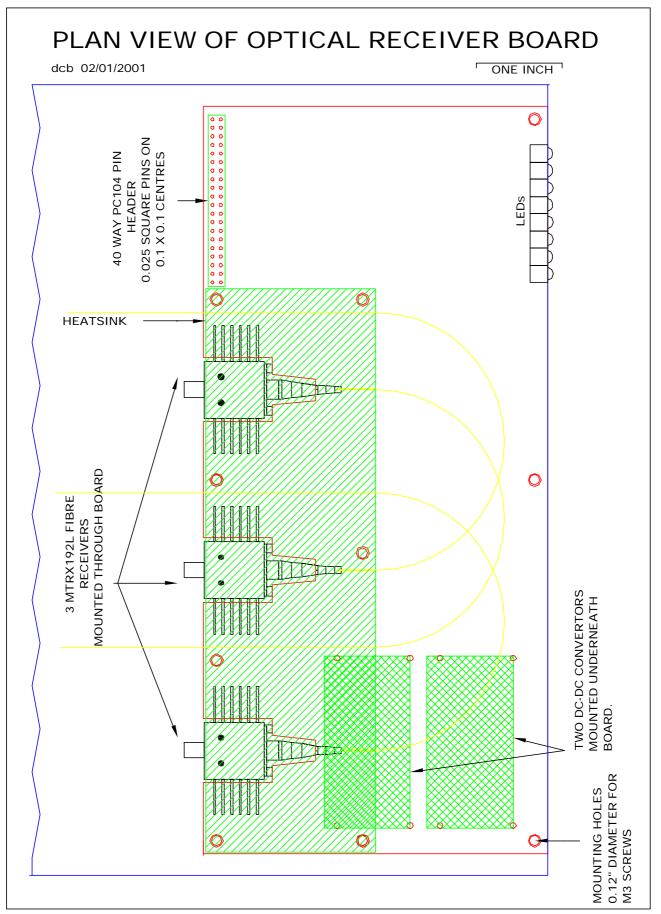


# 7.1.5 Circuit Diagram 4

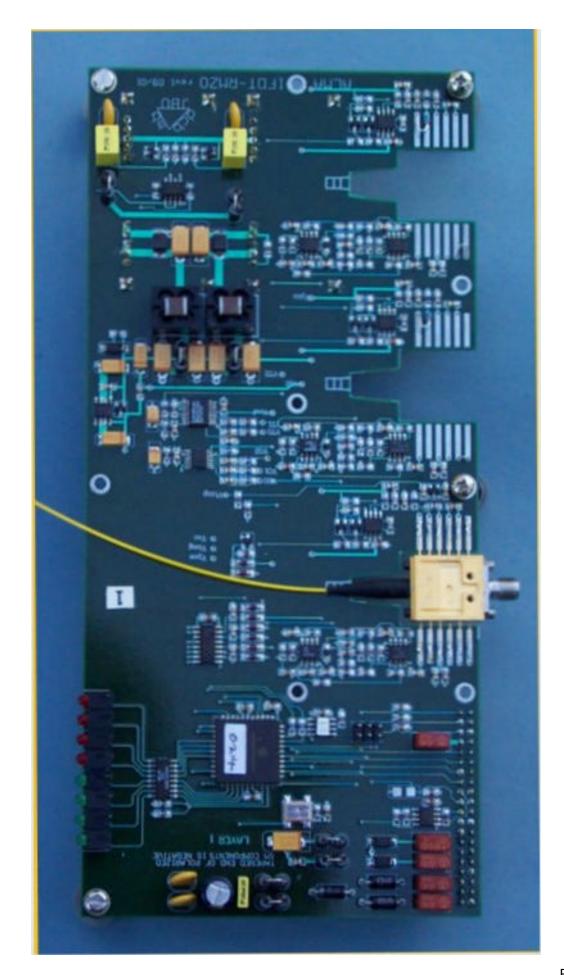




# 7.1.6 Mounting of Optical Receiver Board

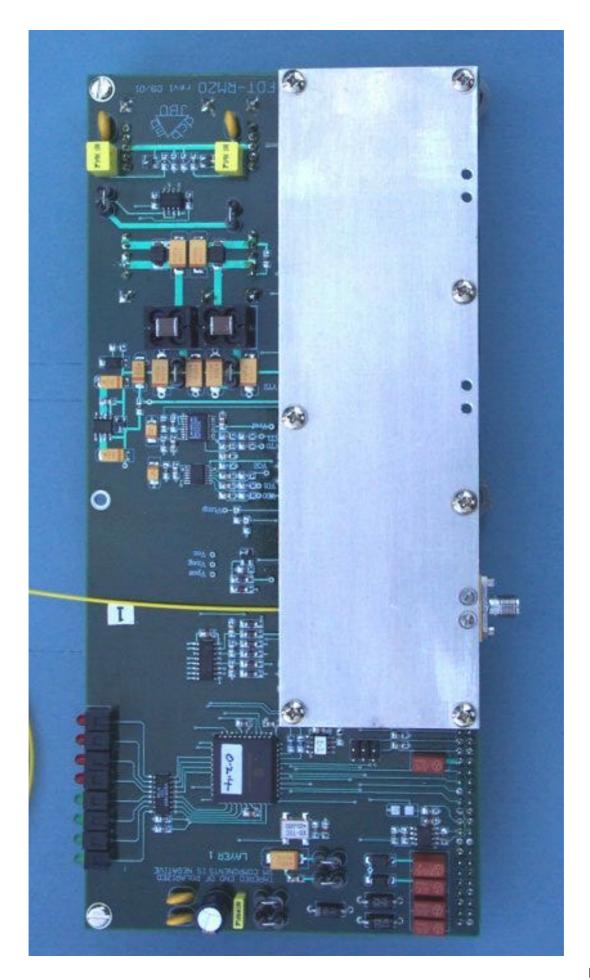


# 7.1.8 Assembly Jig and Heat Sink Mounting

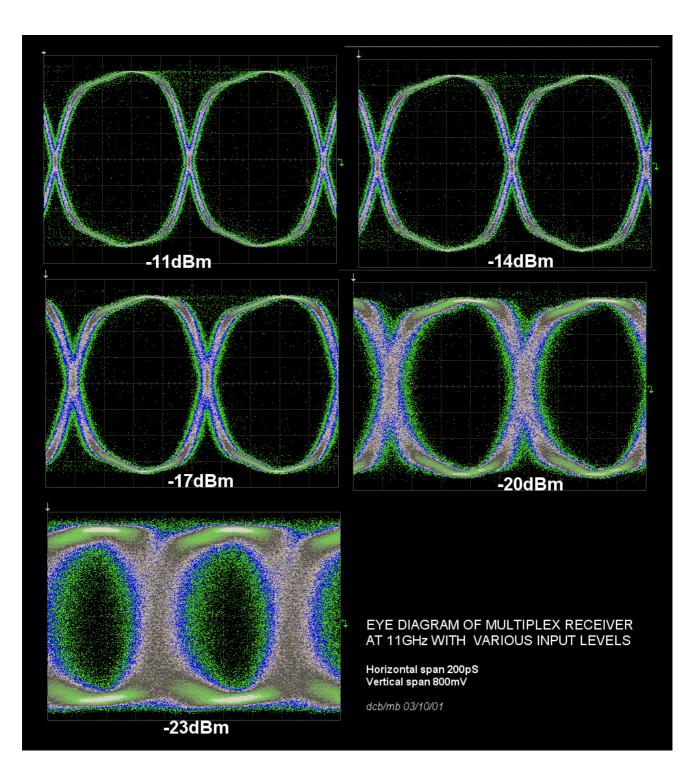


7.2.1 Assembled Board Prior to Fitting Heat Sink

# 7.2.2 Assembled Board with Heatsink



# 7.2.3 Receiver Eye Diagrams



# Appendix B - Firmware For PIC 12C508A

00048

00001 LIST P=12C508A OFFF 001A 00002 CONFIG 0X1A ; MCLR/ enabled - CP off - WDT disabled - internal RC osc 00003 00004 00006 ; These are the sixteen bit serial number to send 00007 00008 #DEFINE SN\_MS 0X10 ; Version number one of board 00009 #DEFINE SN\_LS 0X03 ; Three units built 00010 ; 00012 00013 ; The bit in GPIO which we send it on #DEFINE OUTBIT 0 00014 #DEFINE OPTS 0XBF ; Option to enable weak pull-ups 00015 00016 #DEFINE PW б ; Width of narrow pulse is 3\*PW+7 cycles =25uS 00017 00018 #DEFINE GPIO 0X06 00019 #DEFINE TEMP 0X10 00020 #DEFINE BCNT 0X11 ; Register for counting the pulses 00021 #DEFINE PCNT 0X12 ; Register for counting the pulse width 00022 #DEFINE REG\_MS 0X13 ; Registers to hold the serial number 00023 #DEFINE REG\_LS 0X14 ; 00024 0X15 ; Working registers which store the pulse widths #DEFINE REG\_WI 00025 #DEFINE REG\_NA 0X16 ; 00026 00027 #DEFINE CARRY 0X03,0 ; Carry is bit zero of status register 00028 #DEFINE OSCAL 0X05 ; Oscillator calibration register 00029 00031 0000 00032 ORG 0 00033 0000 0025 00034 MOVWF OSCAL ; Calibrate the oscillator 0CBF 0001 00035 MOVLW OPTS ; Configure the options 0002 0002 00036 OPTION 00037 0003 0506 00038 BSF GPIO, OUTBIT ; Configure the TriState Register so one bit is an output 0004 0070 00039 CLRF TEMP ; and the bit is set 0005 0510 00040 BSF TEMP, OUTBIT 0250 00041 0006 COMF TEMP,W 0007 0006 00042 TRIS 6 00043 0008 0C03 00044 MOVLW SN LS ; Load serial number to registers 0009 0034 00045 MOVWF REG\_LS A000 0C10 00046 MOVLW SN MS 000B 0033 00047 MOVWF REG\_MS

000C	0C10	00049	MOVLW	10	; Load bit counter
000D	0031	00050	MOVWF	BCNT	
		00051			
000E	0C06	00052	MOVLW	PW	; Pulse width in W
000F	0036	00053	MOVWF	REG_NA	; Pulse width in REG_NA
0010	0035	00054	MOVWF	REG_WI	
0011	0403	00055	BCF	CARRY	
0012	0375	00056	RLF	REG_WI,F	
0013	0375	00057	RLF	REG_WI,F	; Four times pulse width in REG_WI
		00058			
0014		00059 LOOP:			
0014	0406	00060	BCF	GPIO,OUTBIT	; Start the pulse
		00061			
0015	0374	00062	RLF	REG_LS,F	; Shift code word left by one
0016	0373	00063	RLF	REG_MS,F	; putting top bit in Carry
0017	0000	00064	NOP		
		00065			
0018	0216	00066	MOVF	REG_NA,W	
0019	0703	00067	BTFSS	CARRY	; Test top bit of code word
001A	0215	00068	MOVF	REG_WI,W	; If clear wide pulse time to PCNT
001B	0032	00069	MOVWF	PCNT	; If set narrow pulse time to PCNT
		00070			
001C	02F2	00071 LAB1:	DECFSZ	PCNT,F	; Delay loop of 3*6=18uS or 3*24=72uS
001D	OA1C	00072	GOTO	LAB1	; adds to previous 7uS
		00073			
001E	0506	00074 BP:	BSF	GPIO,OUTBIT	; Stop pulse – start gap
		00075			
001F	0216	00076	MOVF	REG_NA,W	
0020	0603	00077	BTFSC	CARRY	; Test top bit of code word again
0021	0215	00078	MOVF	REG_WI,W	; If set wide pulse time to PCNT
0022	0032	00079	MOVWF	PCNT	; If clear narrow pulse time to PCNT
		00080			
0023	02F2	00081 LAB0:	DECFSZ	PCNT, F	; Delay loop of 3*6=18uS or 3*24=72uS
0024	0A23	00082	GOTO	LAB0	; adds to previous 4uS and following 3uS
		00083			
0025	02F1	00084	DECFSZ	BCNT,F	; Count 16 pulses in BCNT
0026	0A14	00085	GOTO	LOOP	
0005	0.7.07	00086		D.0117	
0027	0A27	00087 DONE:	GOTO	DONE	; Our small but vital task is done and we
		00088			; may rest content awaiting the next call
		00089 00090	END		
		00090	END		

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

All other memory blocks unused.

Program Memory Words Used:40Program Memory Words Free:472

#### Revision: 0