
ASTRON
UniBoard
bringing radio telescope digital processing to the next level

New techniques open new possibilities: eVLBI

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JIVE NGC

(Next Generation Correlator)

- 10 GbE links from Telescopes
- 2 GHz Analog BW
- 32 Dual Polarized Inputs

The RadioNET FP7 UniBoard Research Activity

- RadioNet FP7 is a European program for radio astronomy
- Several joint Research Activities one of which is UniBoard

- UniBoard lead is by Jive (Arpad Szomoru), board design by Astron, firmware design by Jive, Astron and UniBoard users.

Contract no. 227290

Main Applications Driving the UniBoard

The main performance requirements regarding IO, processing and memory come from:

- EVN2015 correlator (JIVE)
- APERTIF beamformer (ASTRON)
- APERTIF correlator (ASTRON)

EVN2015 Correlator

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APERTIF Focal Plane Array at WSRT

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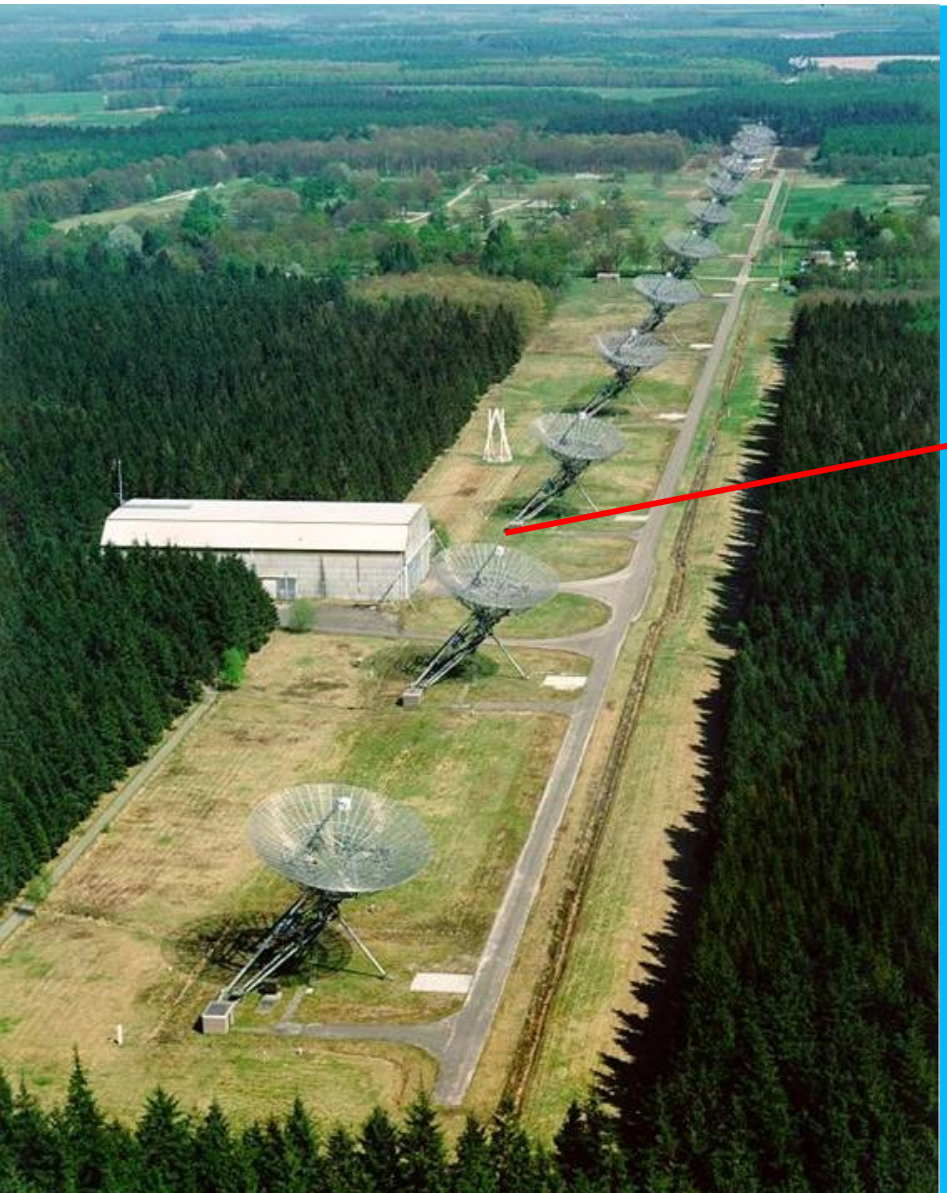

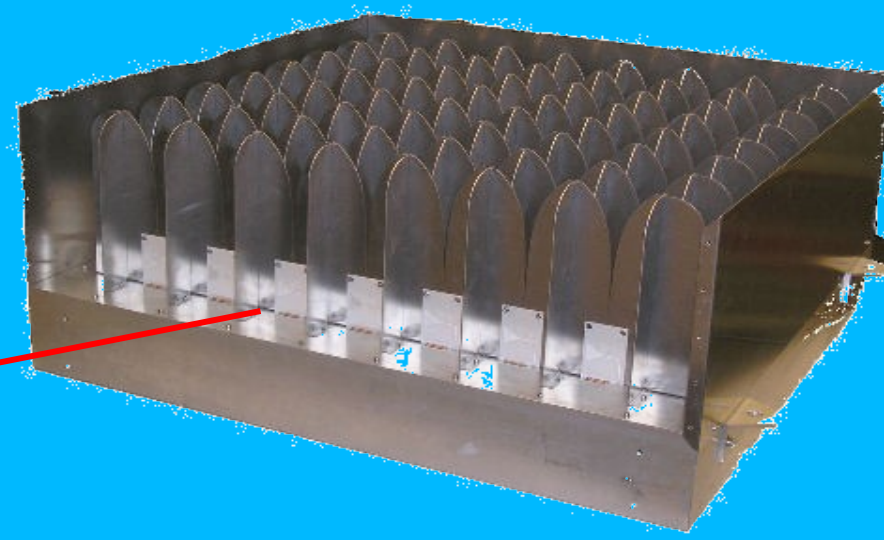

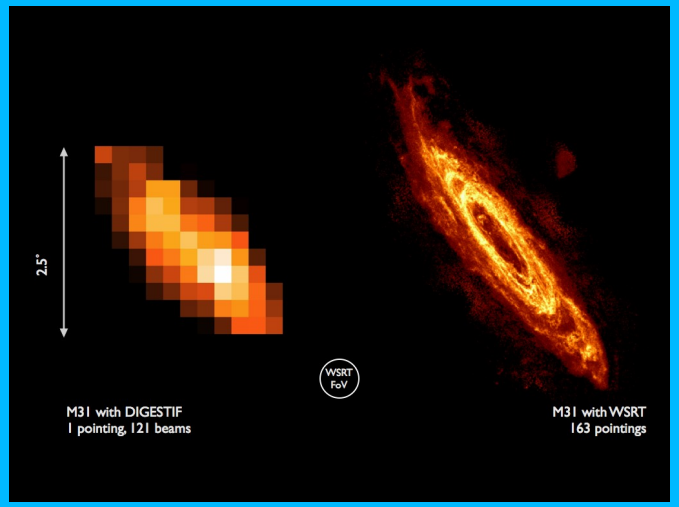

APERTIF Requirements

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- Beamformer:
  - 12 Westerbork 25 m dishes each with a Focal Plane Array
  - 60 dual polarization antennas per telescope
  - 400 MHz RF input bandwidth
  - 300 MHz beam output bandwidth
  - 37 beams

- Correlator:
  - 12 dual polarization FPA telescopes
  - 37 beams, so in total 11000 visibilities

What did we learn from LOFAR

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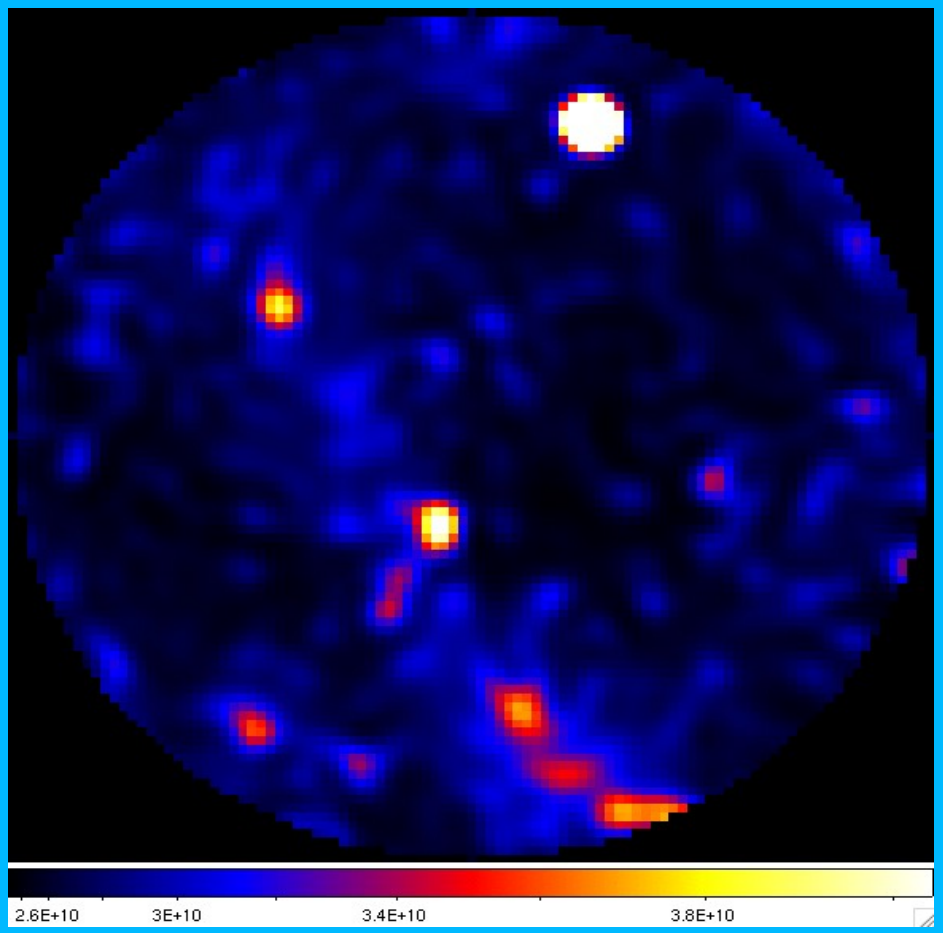
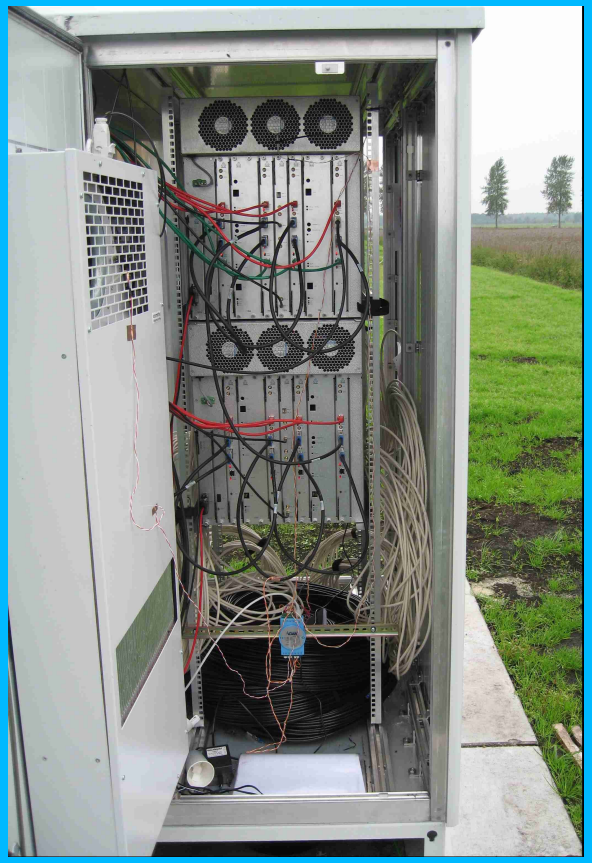
- Don't forget whom you are making systems for !



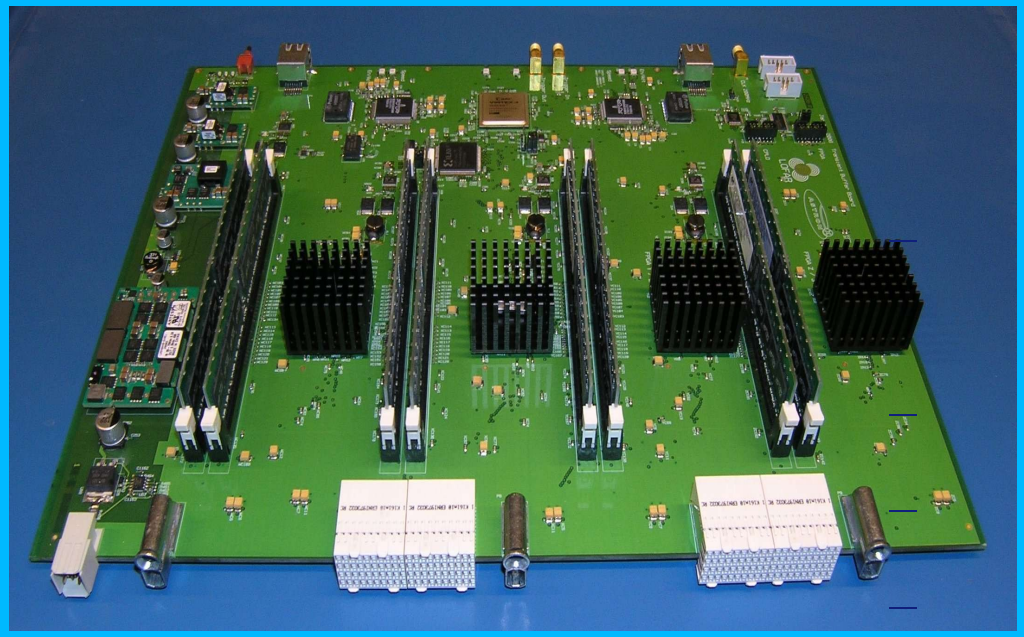
What did we learn from LOFAR

- Try to reduce the number of interconnections



What did we learn from LOFAR

- Close collaboration with production factory
  - what is needed to produce >1000 boards
  - How do you test produced boards



LOFAR Transient Buffer Board

> 10,000 pins

> 2,000 parts

> 1000 DSP-boards in LOFAR

Design Challenges

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Design is a balance between:

- Performance
- Flexibility
- Power consumption
- Development time
- Cost

UniBoard Philosophy

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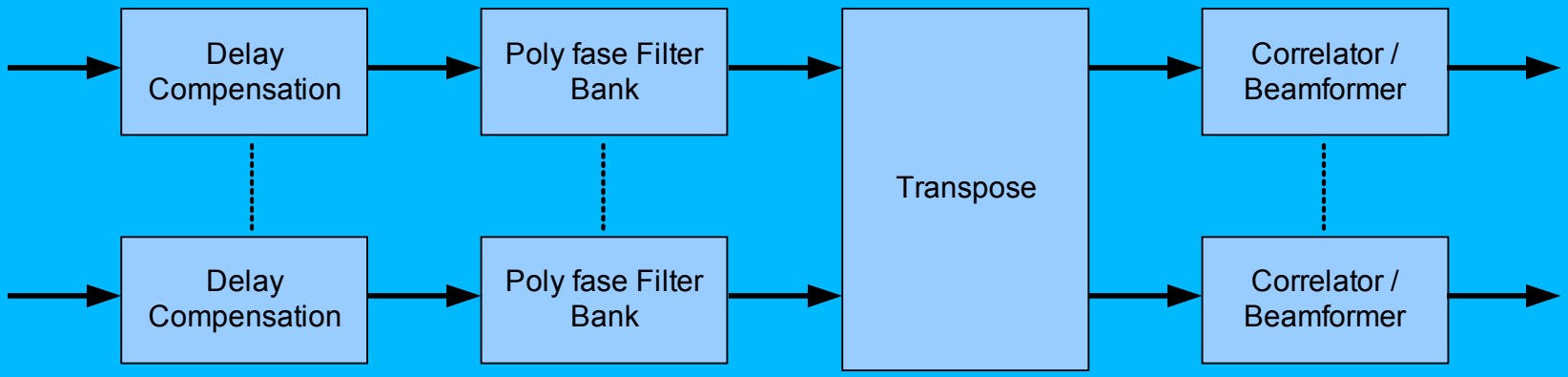
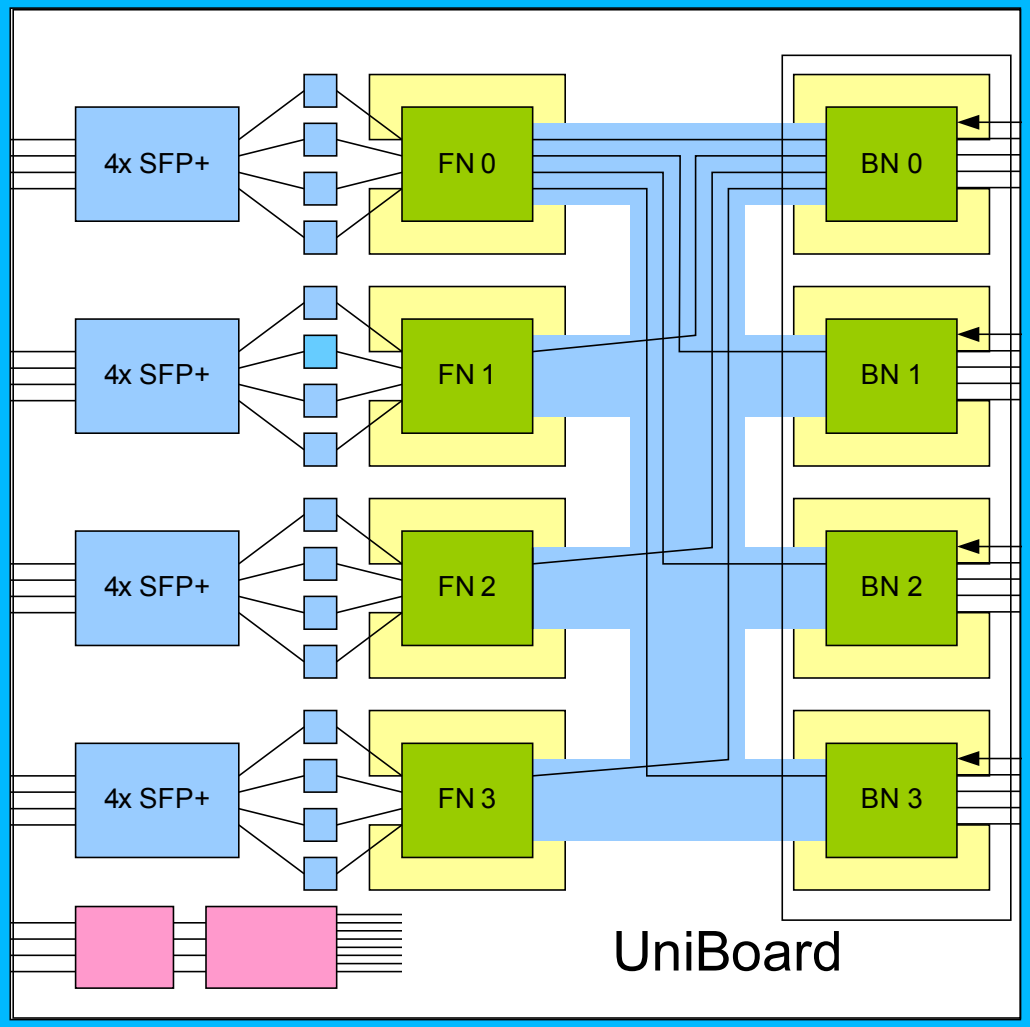
- Continue on the approach we had for LOFAR:
  - High integration density
  - Scalable allowing one, more or many boards
- Use 10GbE interfaces for data IO
- All FPGAs should have the same capabilities
- Minimize overhead
- Usage of one type of board for multiple applications
- The firmware makes the board application specific
- Model Based Design for more rapid application development

Data Path


Delay Compensation
Delay Compensation
Poly fase Filter Bank
Poly fase Filter Bank
Transpose
Correlator / Beamformer
Correlator / Beamformer

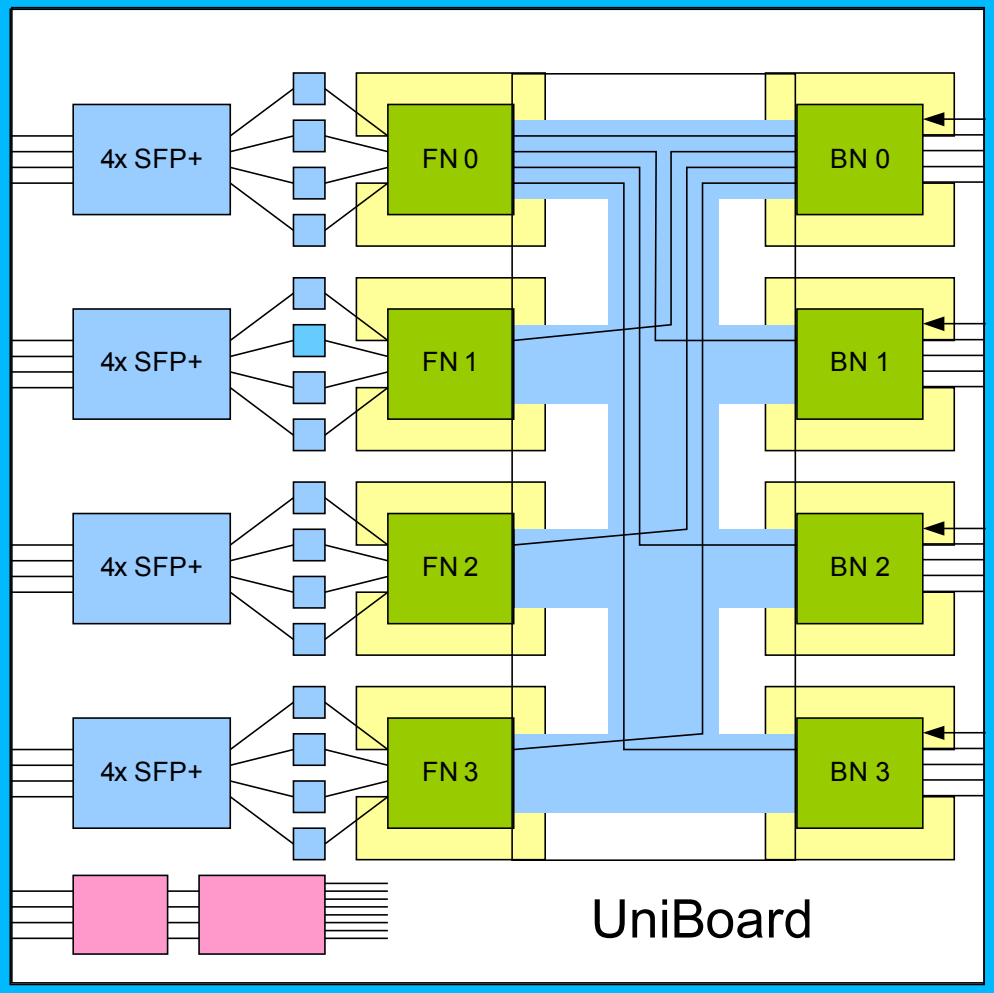
UniBoard used for a Beamformer
Poly Fase Filterbank in Back Nodes (BN)



For Filtering:

- Each BN have 4 8bit interface for ADCs
- Each BN has 2 DDR3 memories
- Multipliers in the FPGAs running at 400MHz

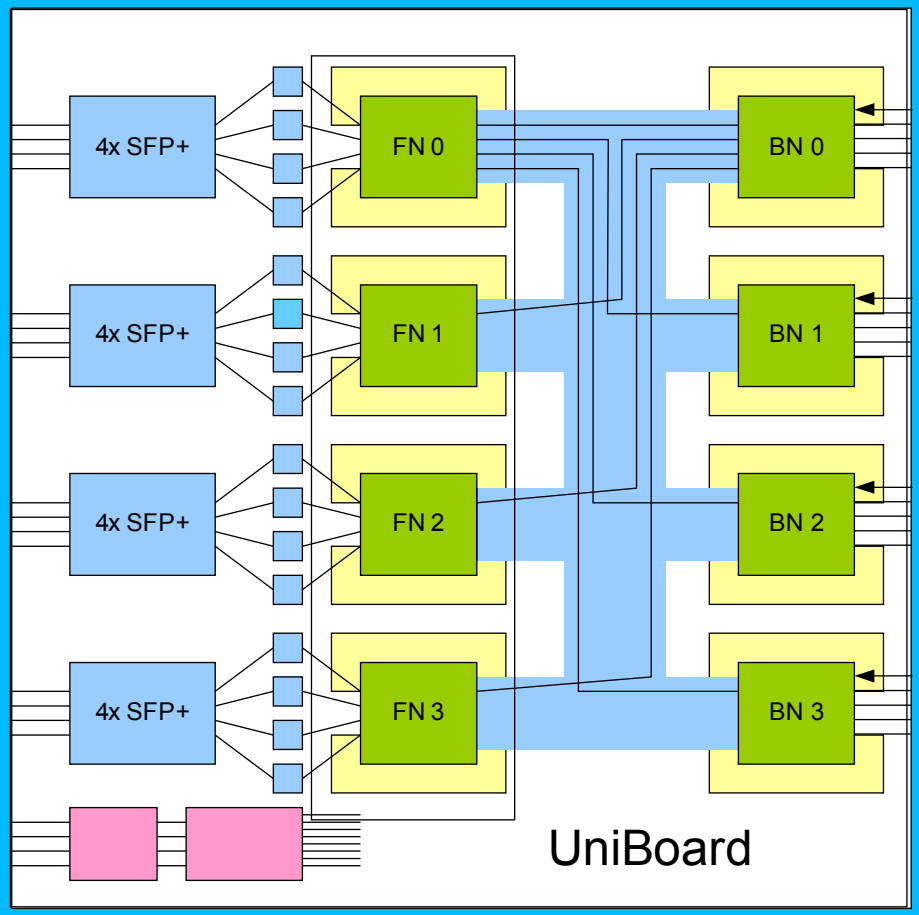
UniBoard used for a Beamformer Transpose on Board



For Transpose:

- Each FN has a 10GbE connection to each BN

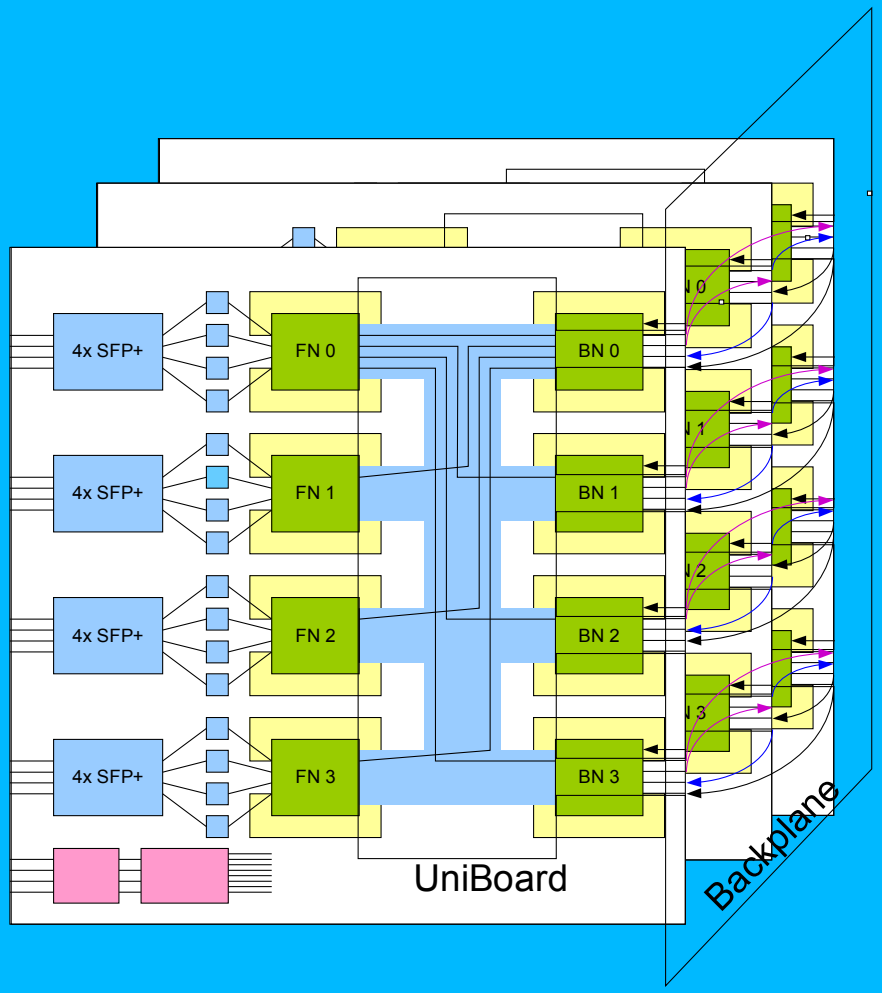
UniBoard used for a Beamformer
Beamforming in Front Nodes (FS)



For Beamforming:

- Front nodes have DDR3 interface for intermediate storage
- FPGA with Multipliers running at 400MHz

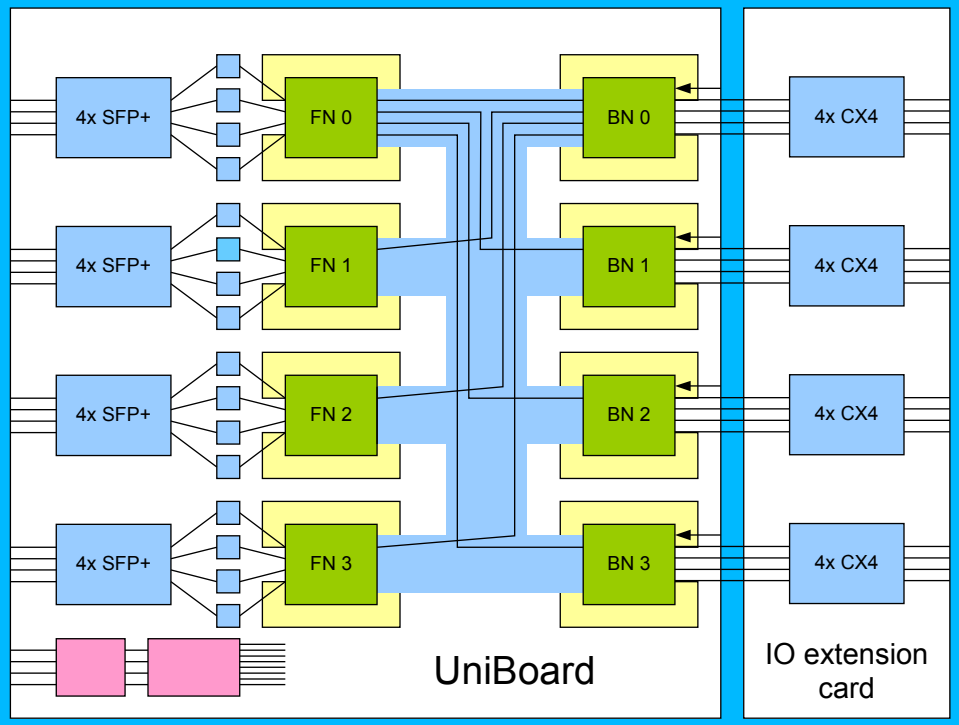
UniBoard used for a Beamformer Transpose partly on Backplane



For large systems:

- Each BN has 4 10GbE F.D. interface to backplane
- 10GbE interfaces can be split into 4 lanes running at 3.125Gbps
- Up to 9 board can be interconnected on a backplane

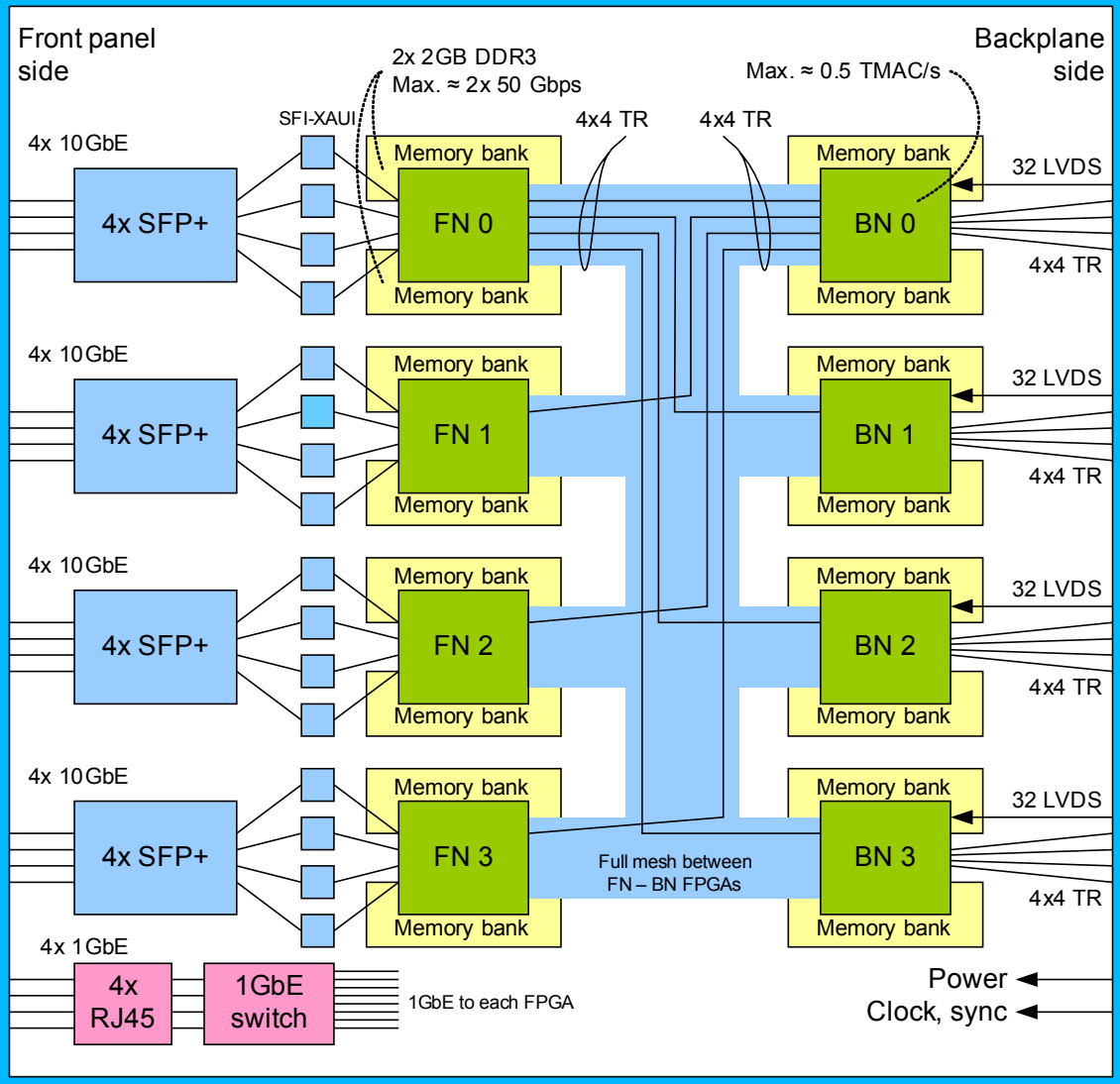
UniBoard with 10GbE IO Extension Card



For smaller systems:

- Instead of a backplane, a interface module can be place. This gives 16 optical/SPF+ interfaces on one side and 16 10GbE CX-4 interfaces on the other side

UniBoard Overview



UniBoard:

- 8 x Altera Stratix IV 40nm FPGA (EP4SGX230KF40)
- 16 x up to 4GByte DDR3 memories
- 16 SFP+ Cage on the input

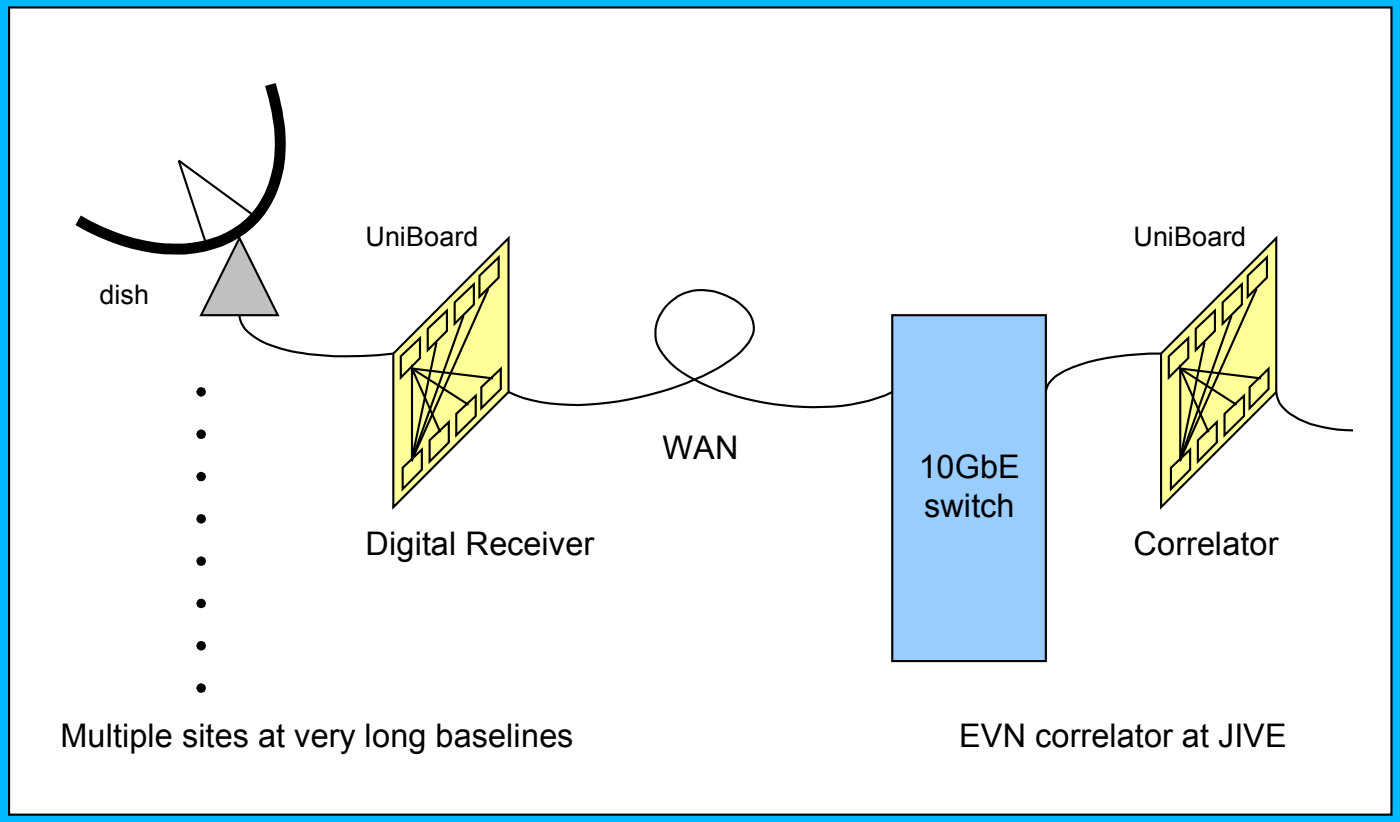
Main Applications Driving the UniBoard

The main performance requirements regarding IO, processing and memory come from:

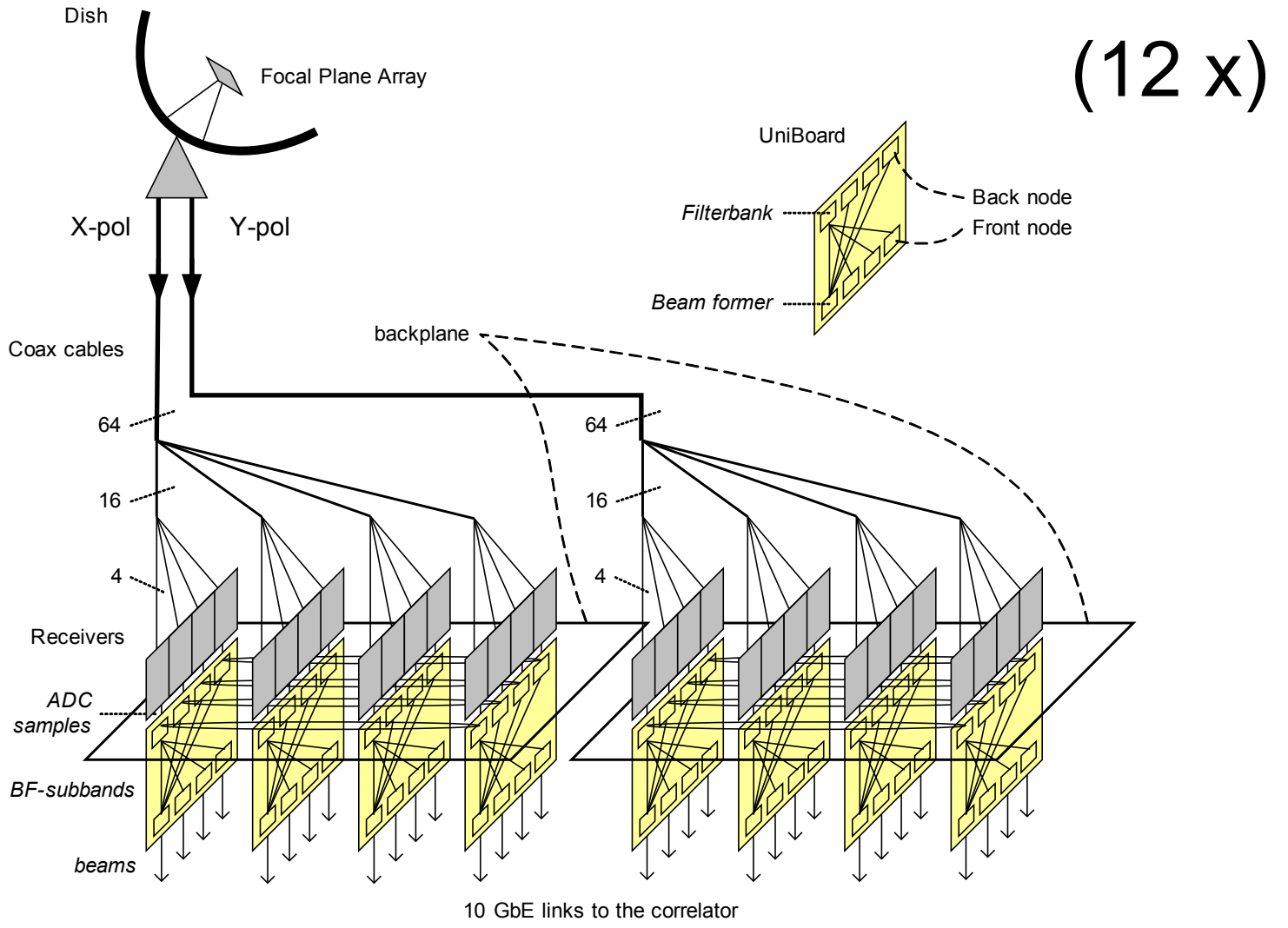
- EVN2015 correlator (JIVE)
- APERTIF beamformer (ASTRON)
- APERTIF correlator (ASTRON)

UniBoard for EVN2015 Correlator

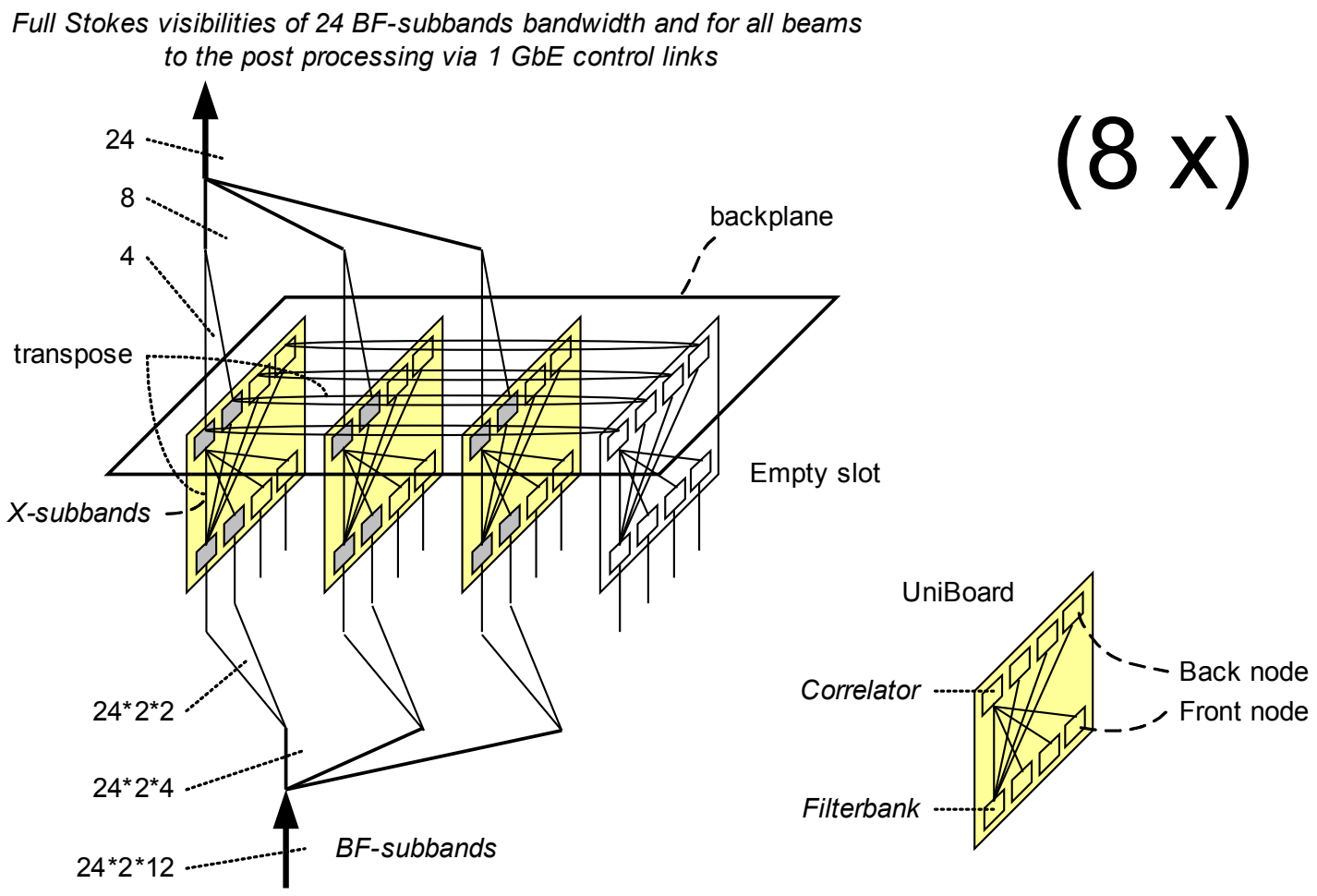
- 32 dual polarization antennas, so 2080 visibilities
- 2 GHz RF input bandwidth



UniBoard for APERTIF Beamformer



UniBoard for APERTIF Correlator



Challenges

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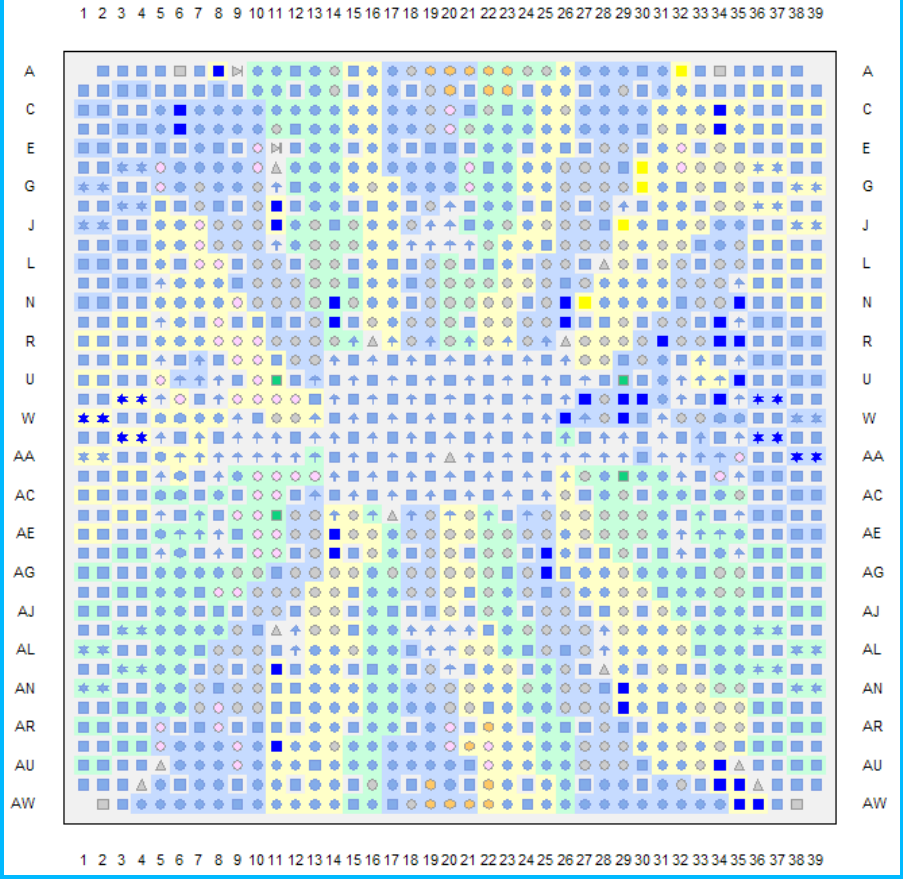
- Data speeds (3.125Gbps / 6.5 Gbps)
- DDR3 interface
- Power

- Fitting the firmware in the Altera devices
- Running at 400MHz clock
- Running the multipliers at full speed
- Storting the data

Used Technologies
FPGA



Altera Stratix IV FPGA

IO

- 2 sides with serial interfaces
- 2 sides for memory

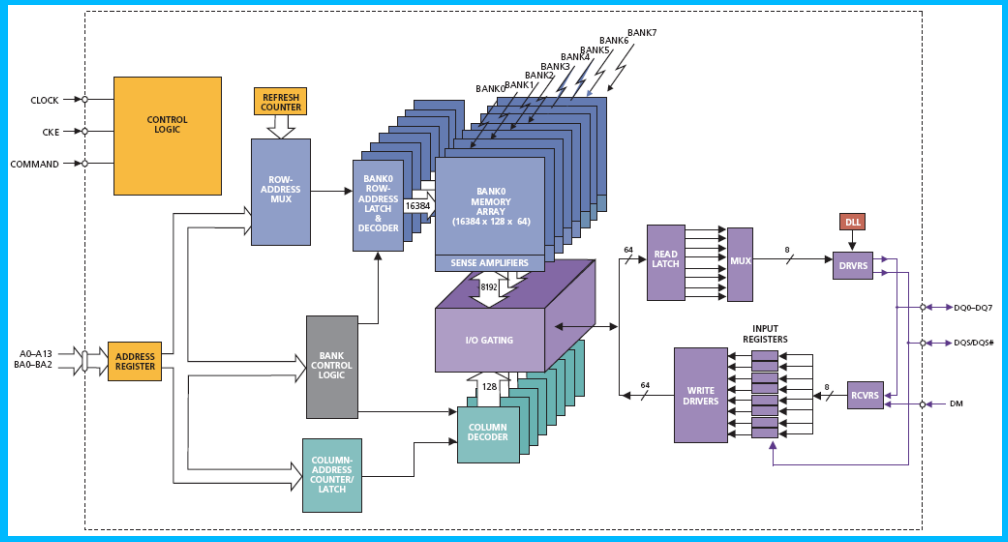
Up to 1288 Multipliers

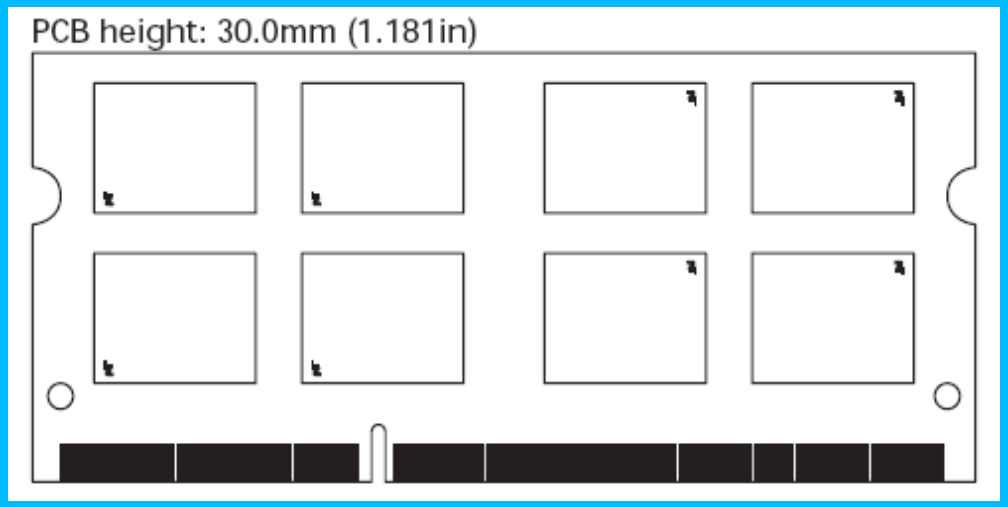
40nm

- less consumption

Multiple parts can be placed on same footprint

Used Technologies
DDR3



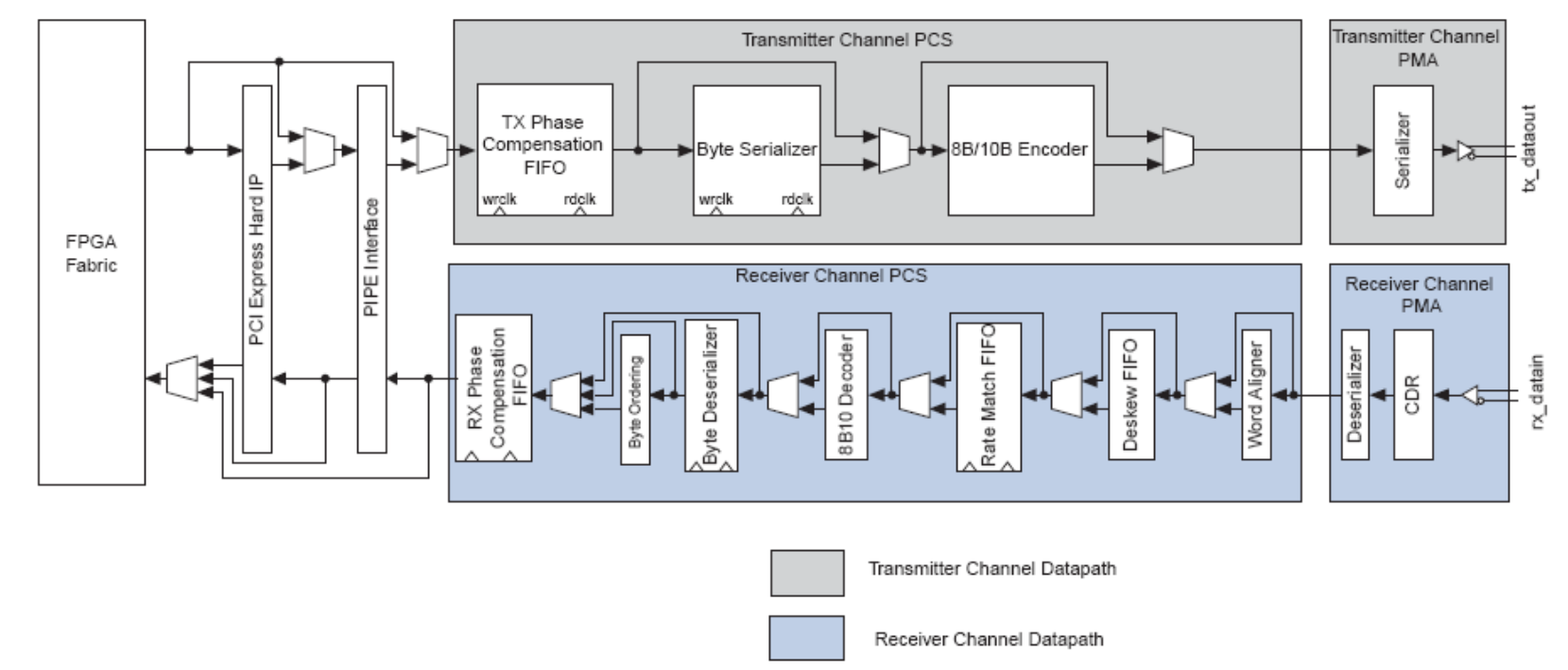


Fast data transfer
- Double Data Rate
- 64 bit ~ 800MT/s

Industry standard
- Easy increase of memory size

SODIMM
- Small board layout

Used Technologies
SerDes



Reduce the number of interfaces by combining multiple low speed interfaces into a single high-speed interface

SerDes included inside FPGA with signal conditioning

Used Technologies
SFP+

- Industry standard
- Optical interfaces
- Copper interface with direct attach

Images Tyco Electronics, see
http://www.tycoelectronics.com

UniBoard Status

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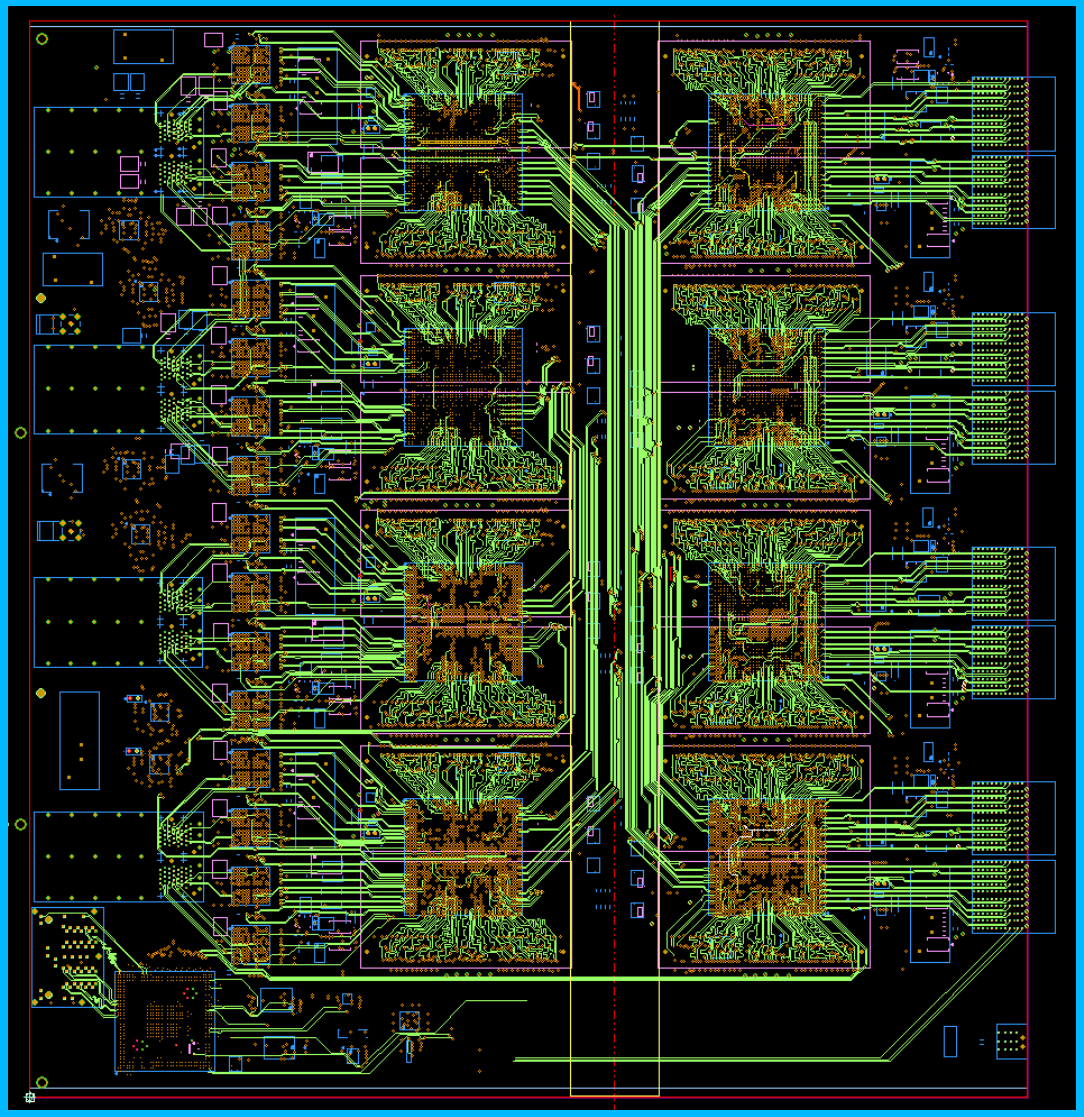
- Schematic design finished and reviewed
- Board manufacturer selected
- Board layout 50% done
- Test firmware writing ongoing
- Model Based Design started

UniBoard Layout ongoing



- H x D x T =
  9HE x 340 x 2.4mm
- 12 layers PCB