

Kris Zarb Adami

Jack Hickish

Richard Armstrong

(jack.hickish@astro.ox.ac.uk)

2-PAD All-Digital Beamforming

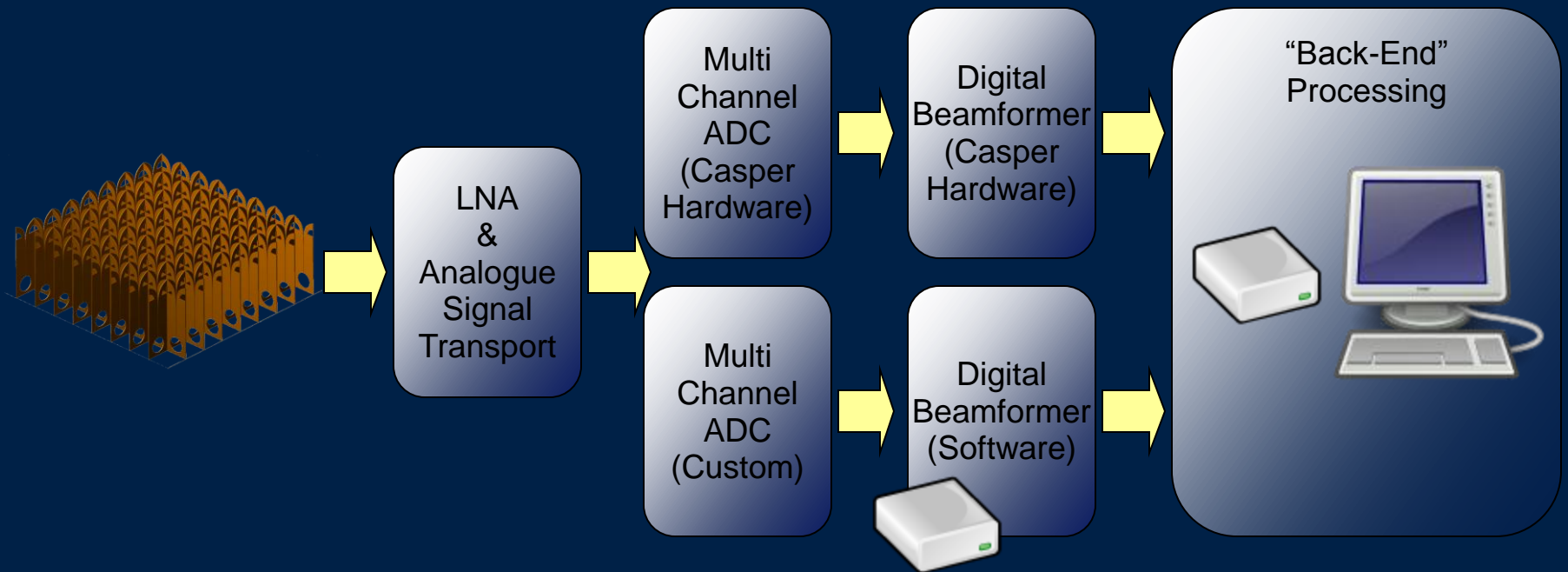


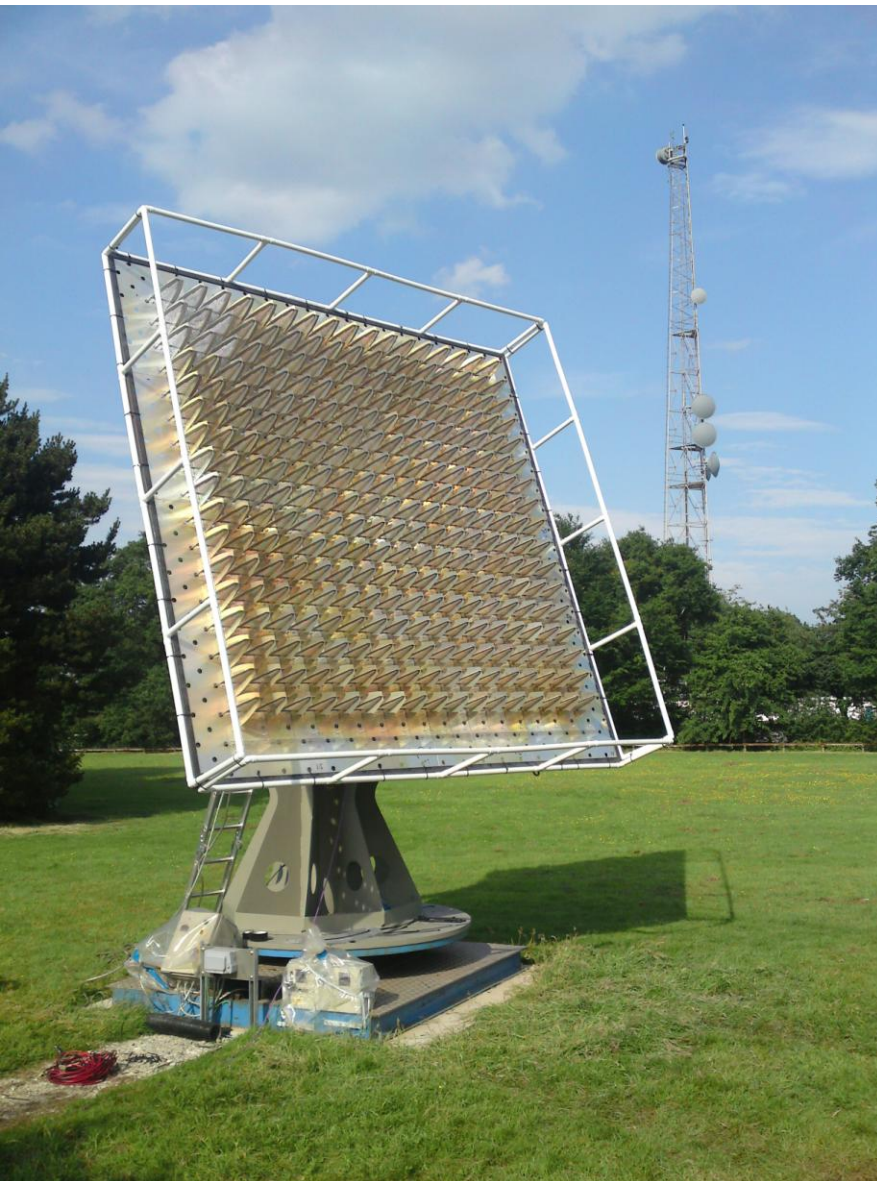
**2PAD current digital
architecture (CASPER)**

**Developing the 2PAD
model**

Future Work

The 2PAD System





200 MHz B/W

**16-dual-pol.
antennas**

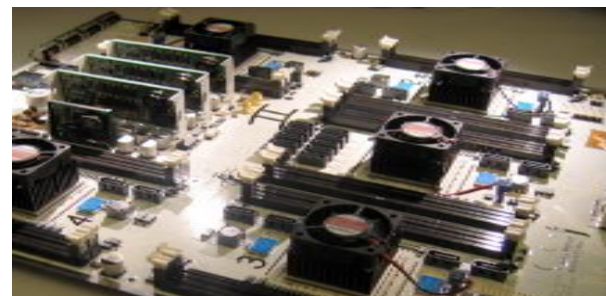
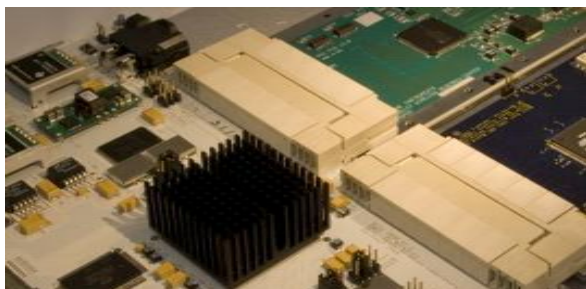
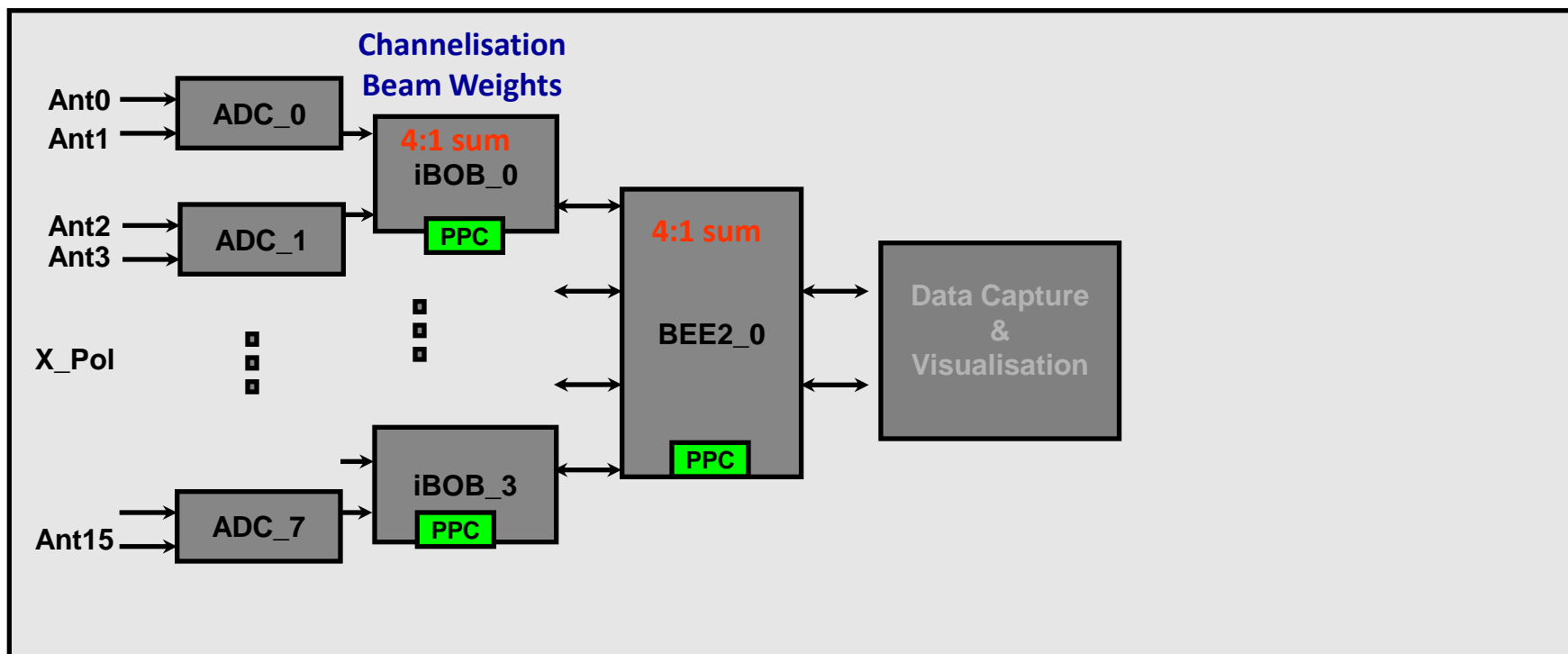
1024

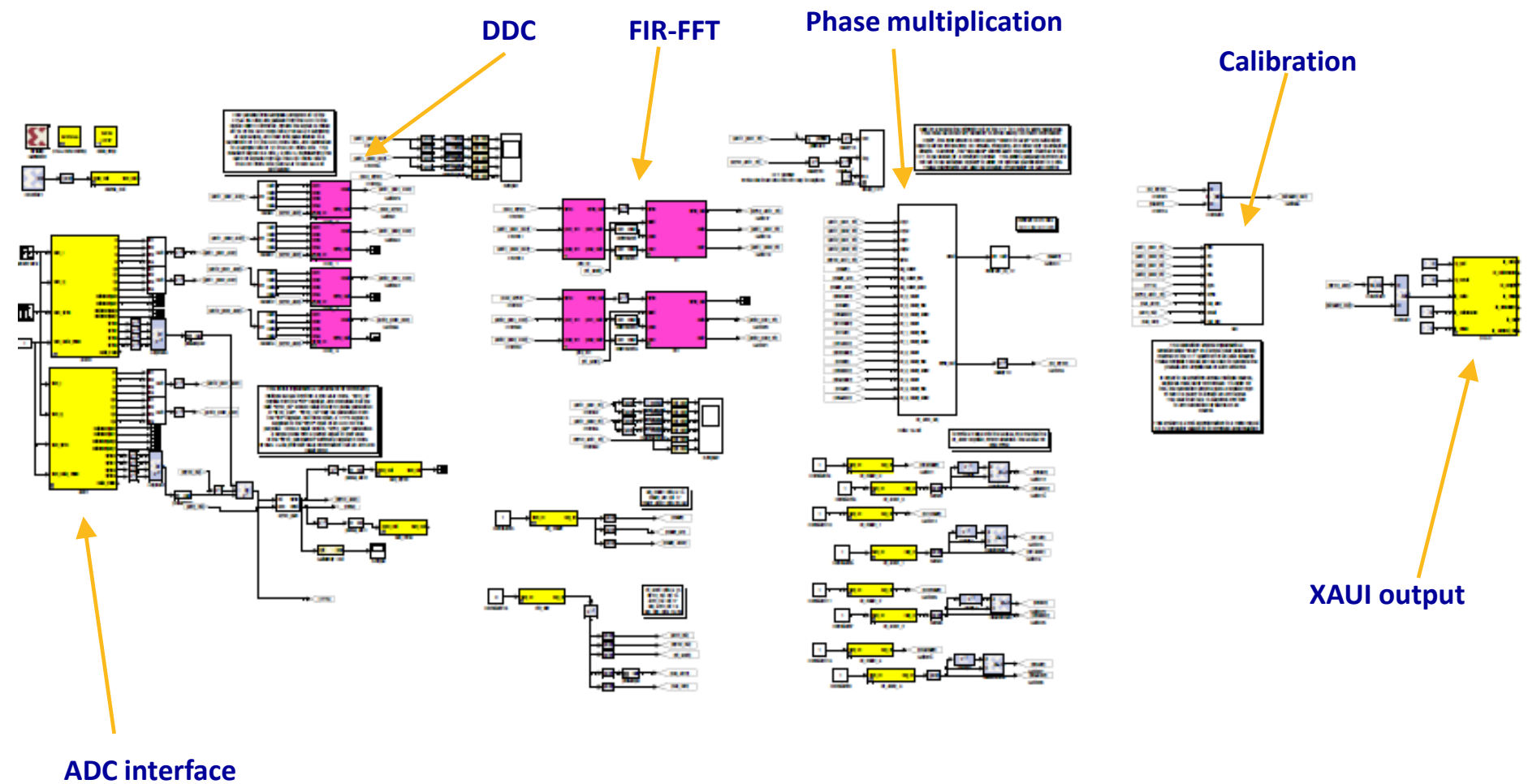
Channels

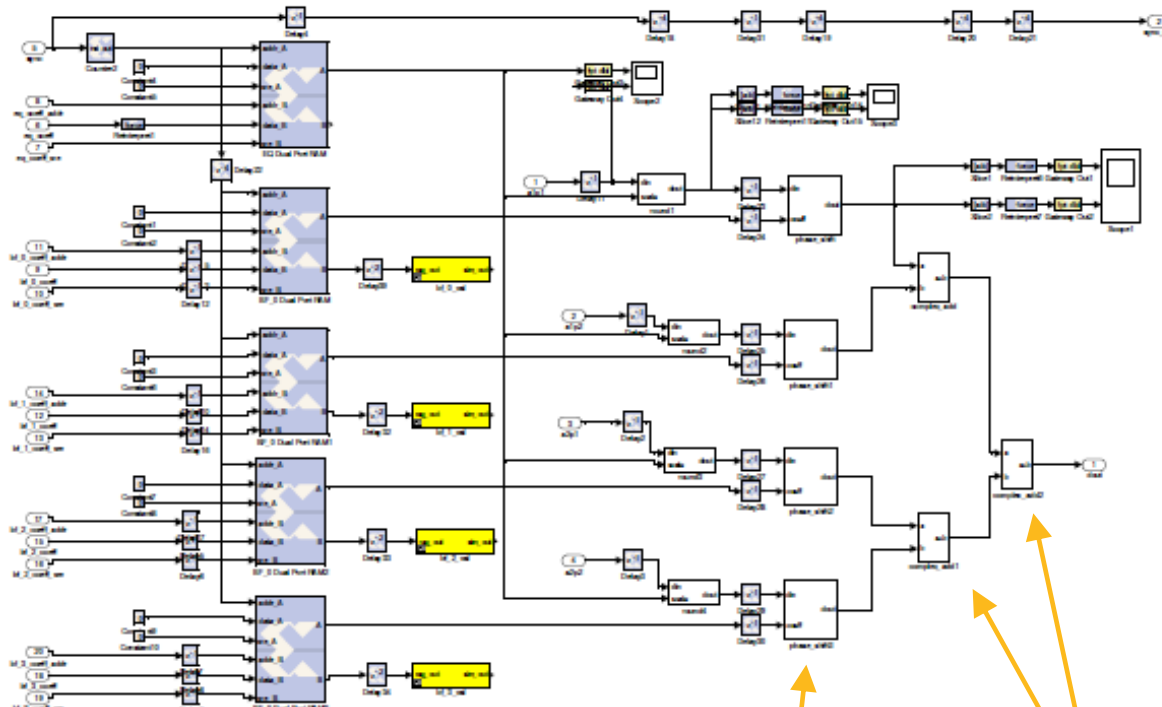
1 Beam

(Virtex-IIP)





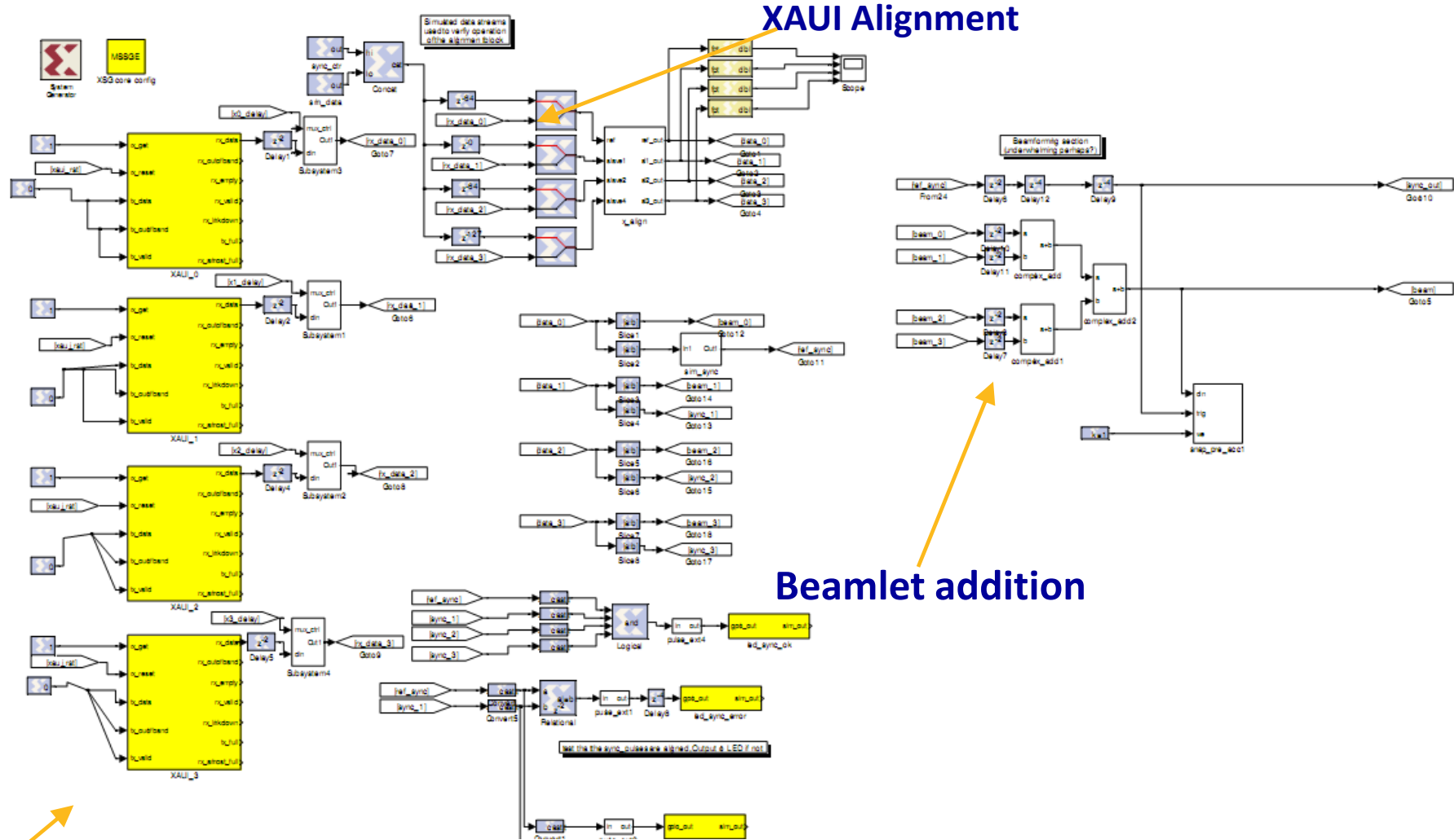


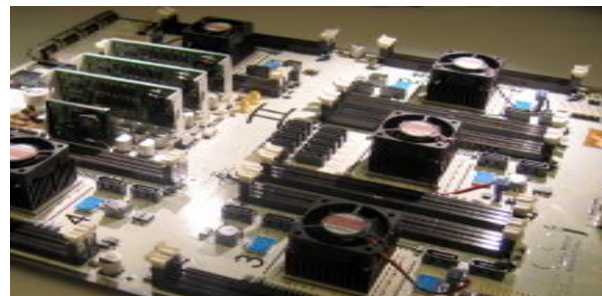
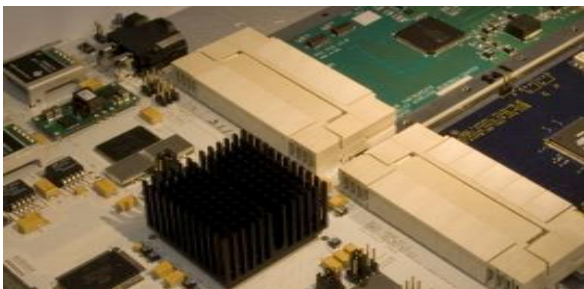
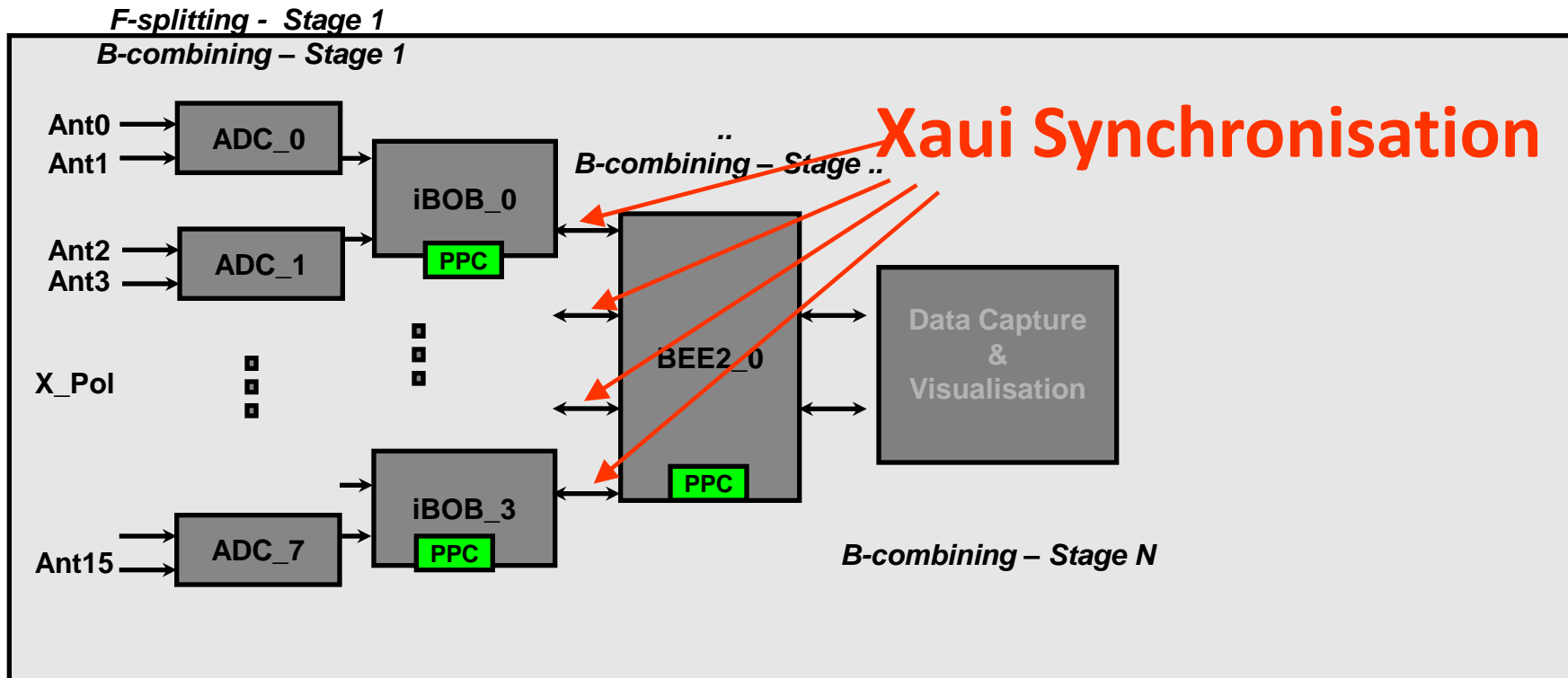


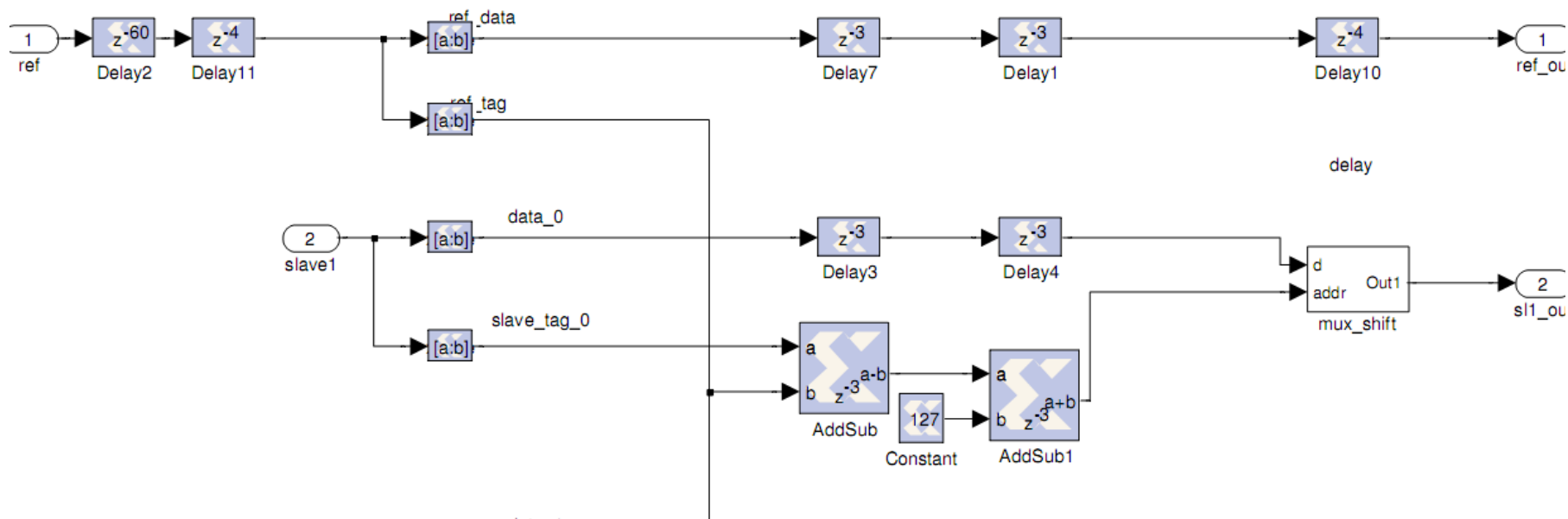
Coefficient bram

Complex multiplier

Complex Adder





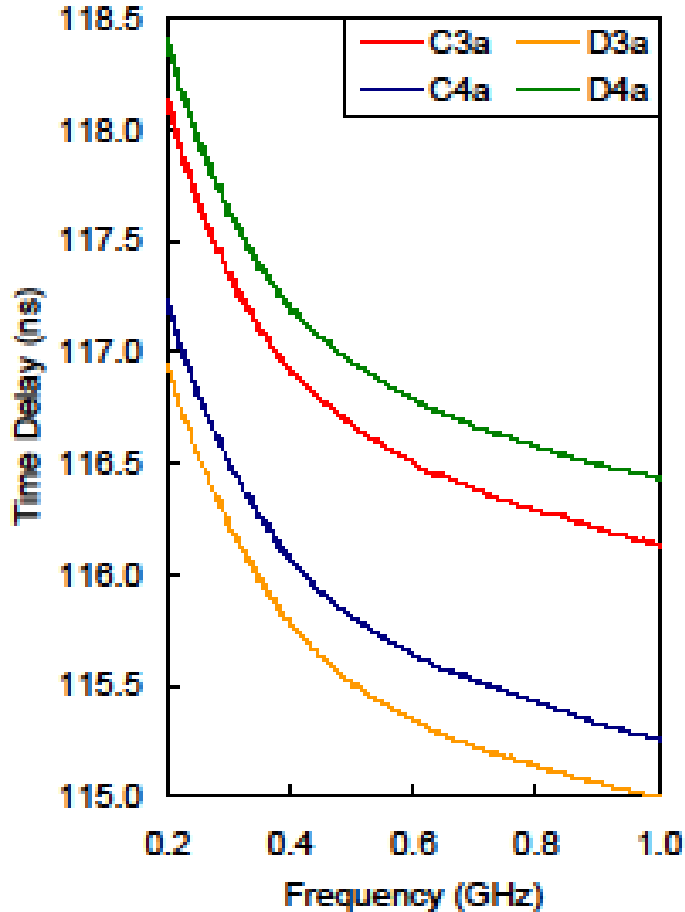


Tag data streams with n bit counter → Allows alignment of $\pm 2^{n-1}$ clocks

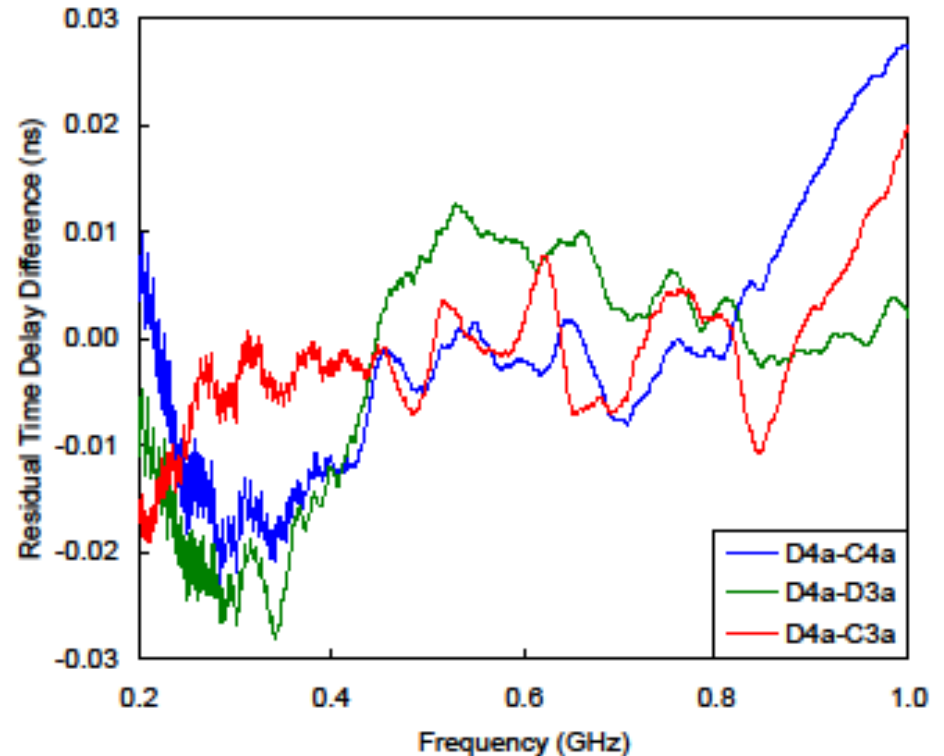


Results

2PAD: delays between 4 analogue channels (D. Price & S. Schediwy, 2009)



Relative delays across band for 4 2PAD channels (Price & Schediwy, 2009)



At 1GHz 0.03ns → 5 degree pointing error [OSKAR Simulator]

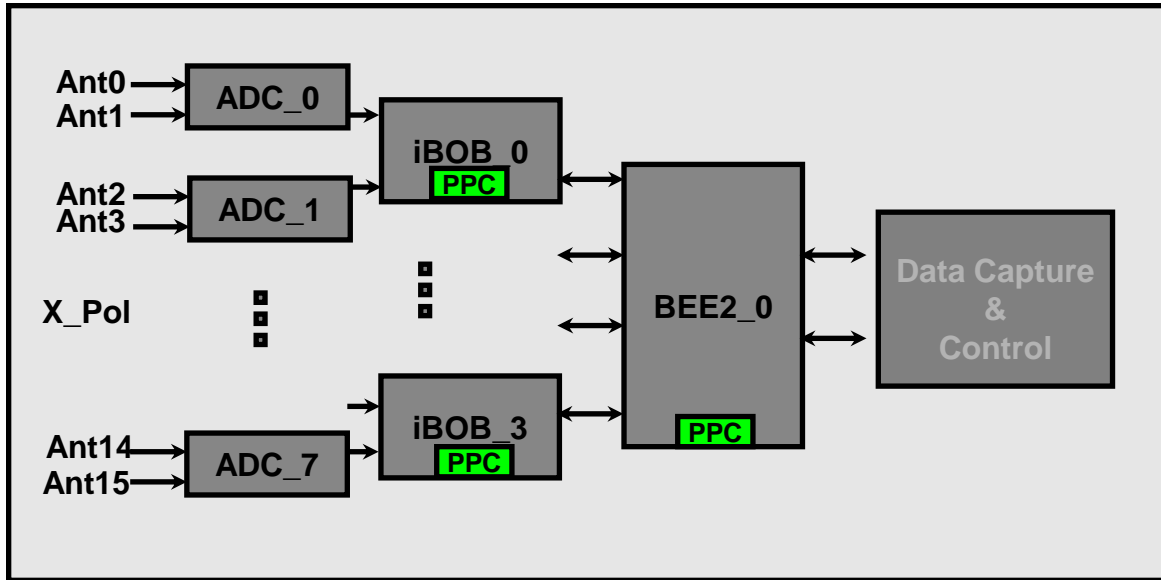


$$X(\omega) = e^{i\phi}$$
$$Y(\omega) = X(\omega)e^{i\theta}$$

Correlation:

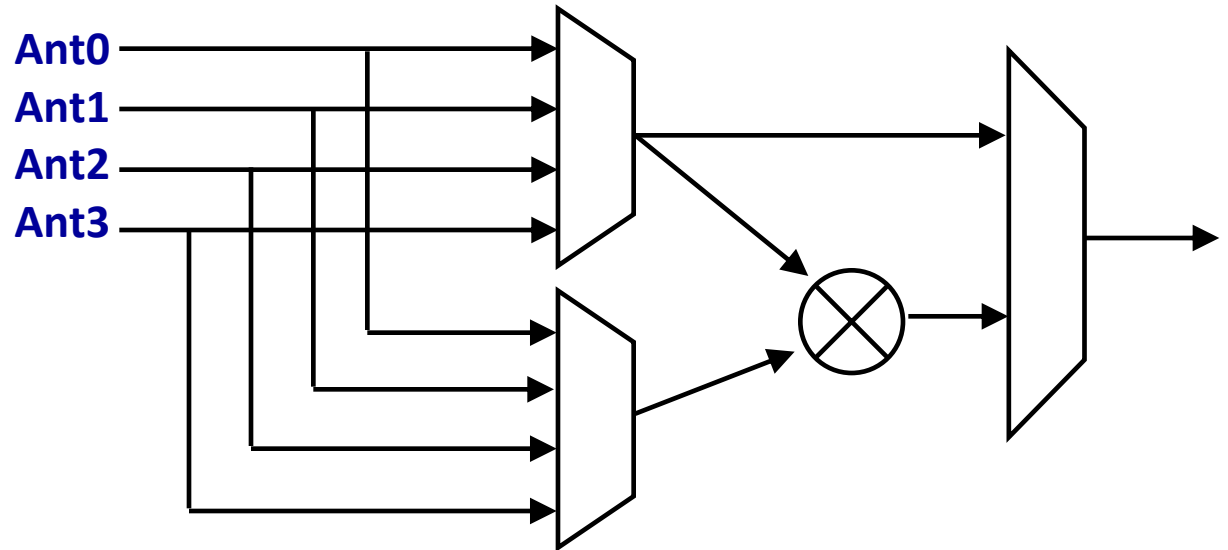
$$Y^*X = |X|^2 e^{-i\theta}$$

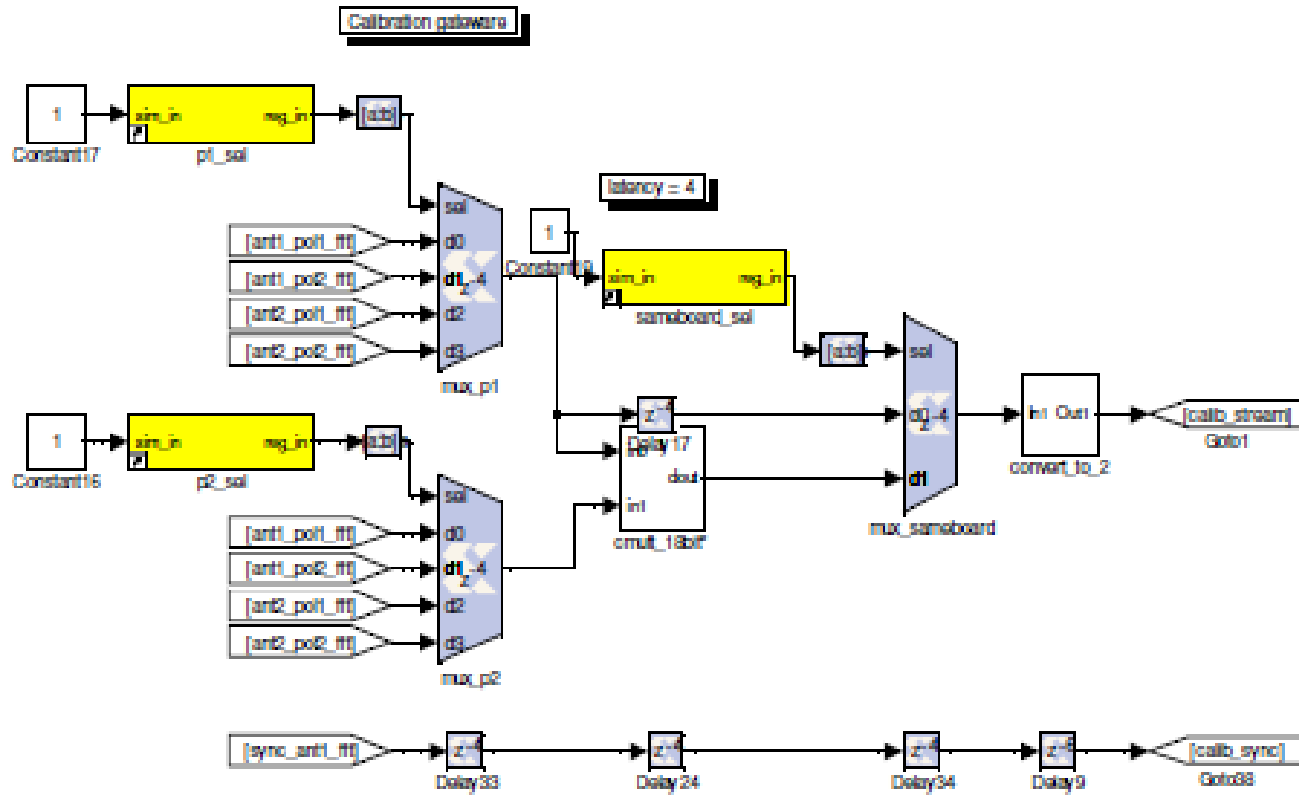
**Beam forming phases are modified
with the phase of the correlation Y^*X**



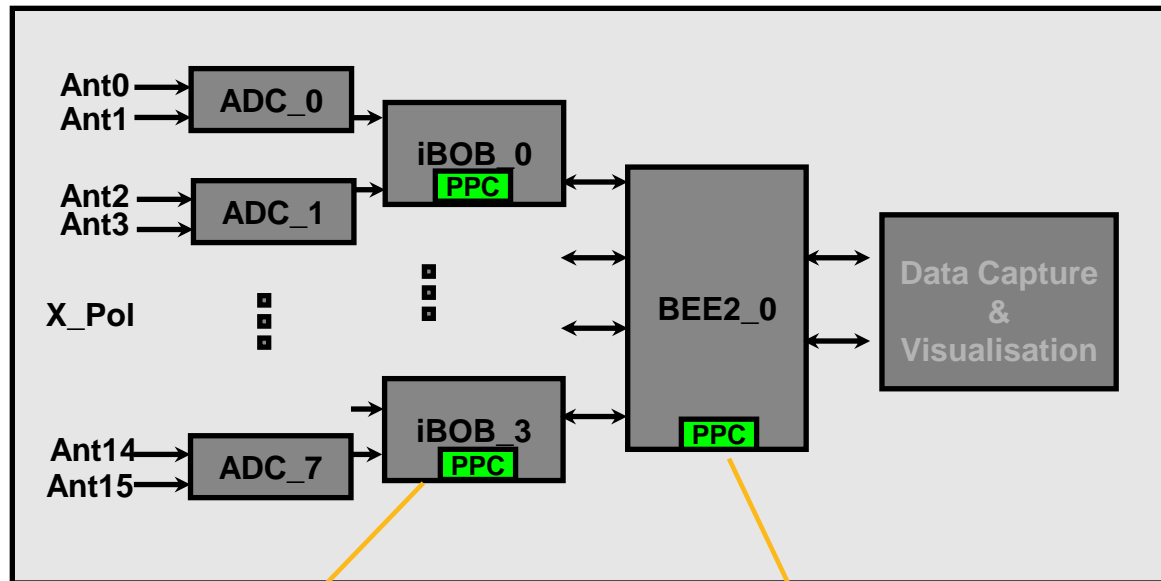
**Time Multiplexed
Nx1 (Potentially
NxN) Correlation**

**iBOB routing
requirements**



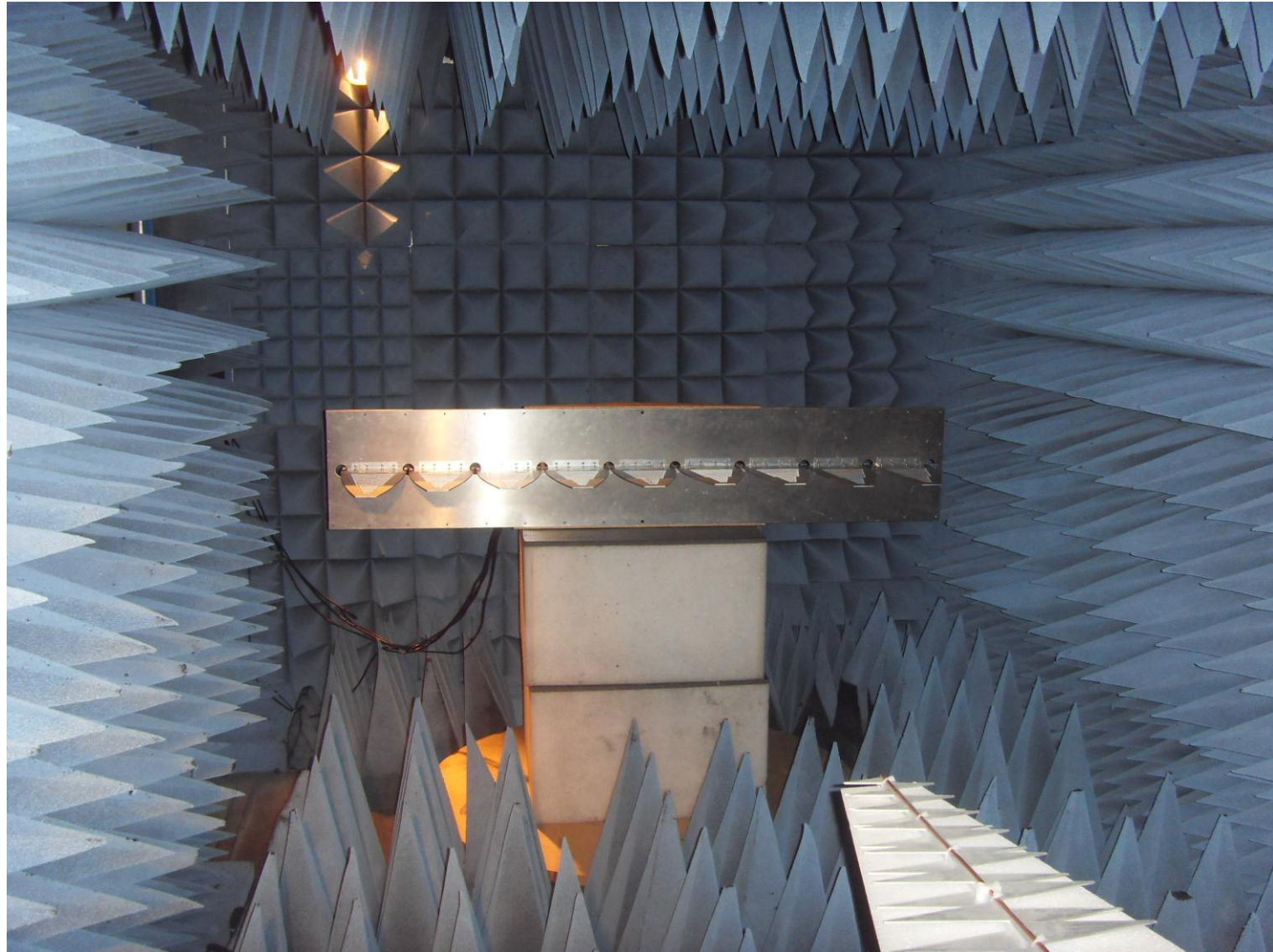


Hierarchical Calibration at board level?

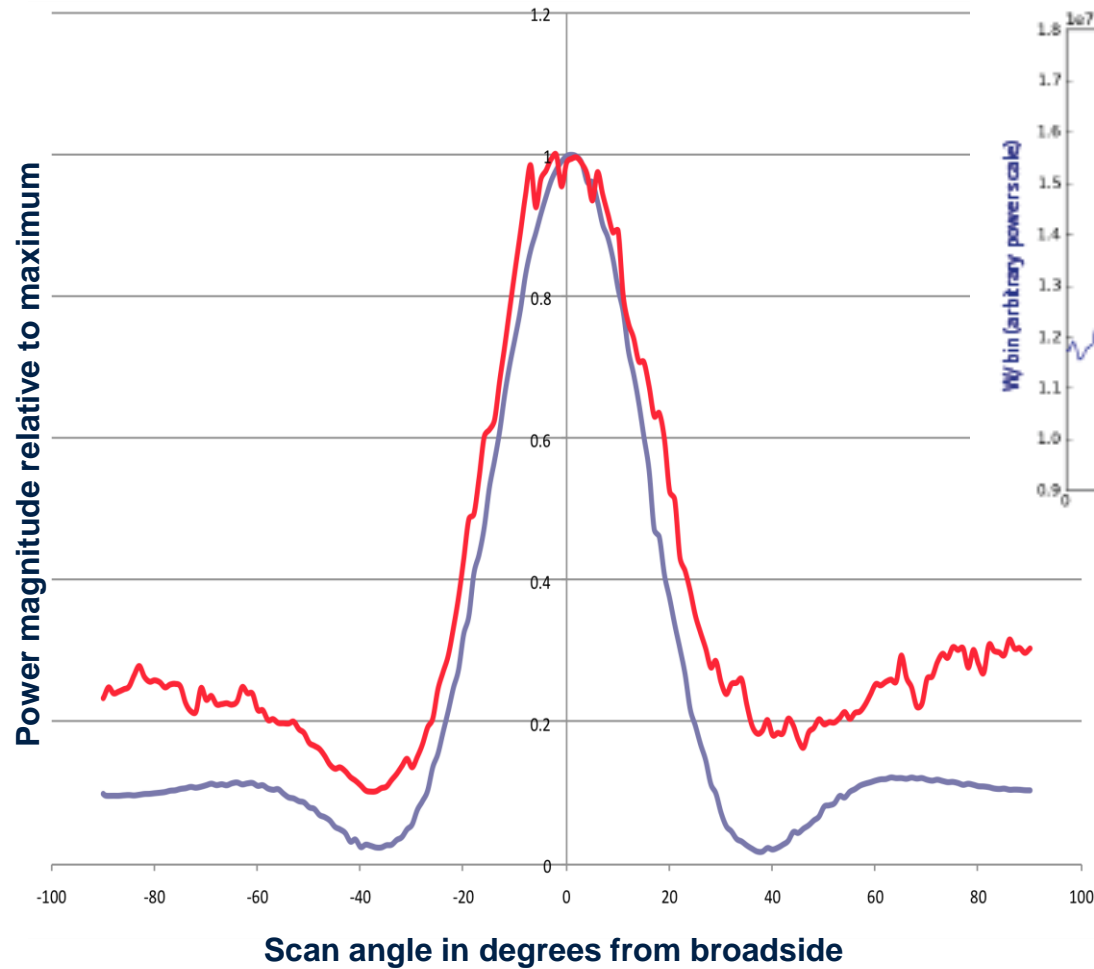


Correlate 4 inputs

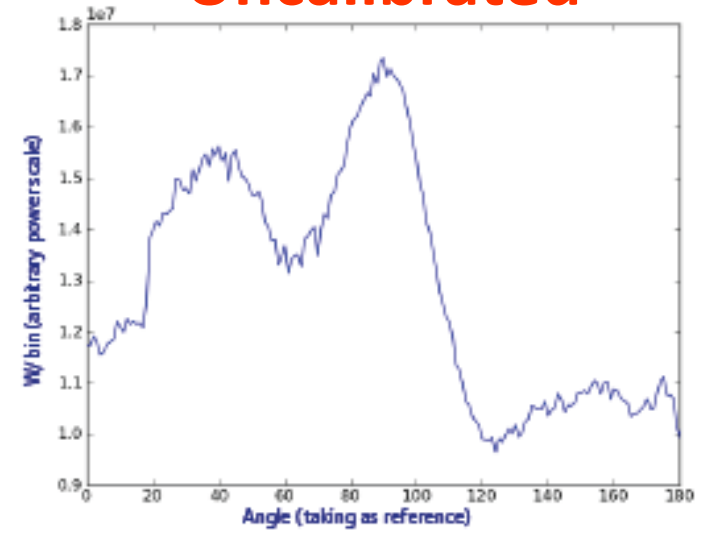
Correlate 4 Beamlets

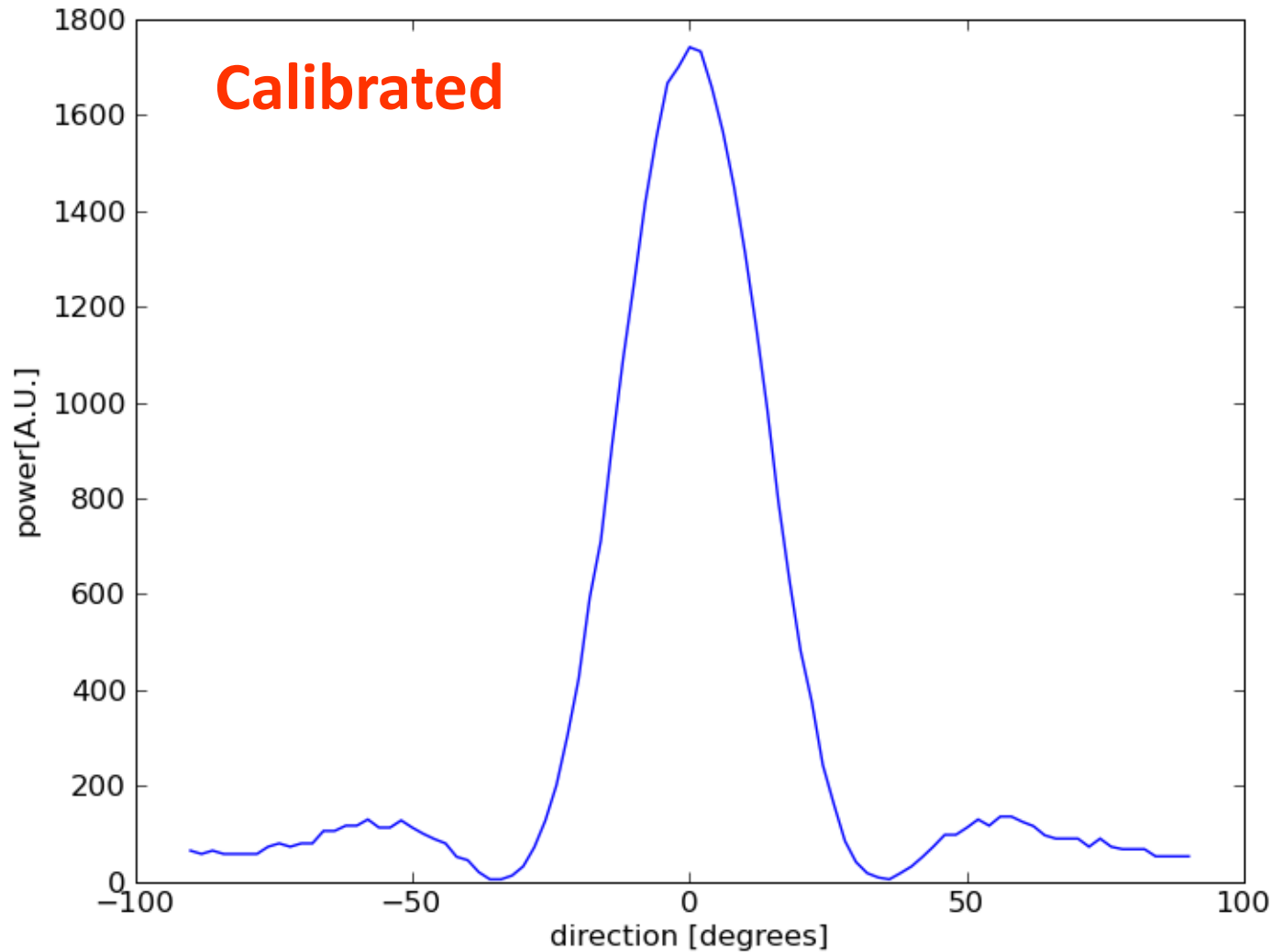


Anechoic vs Field Beam

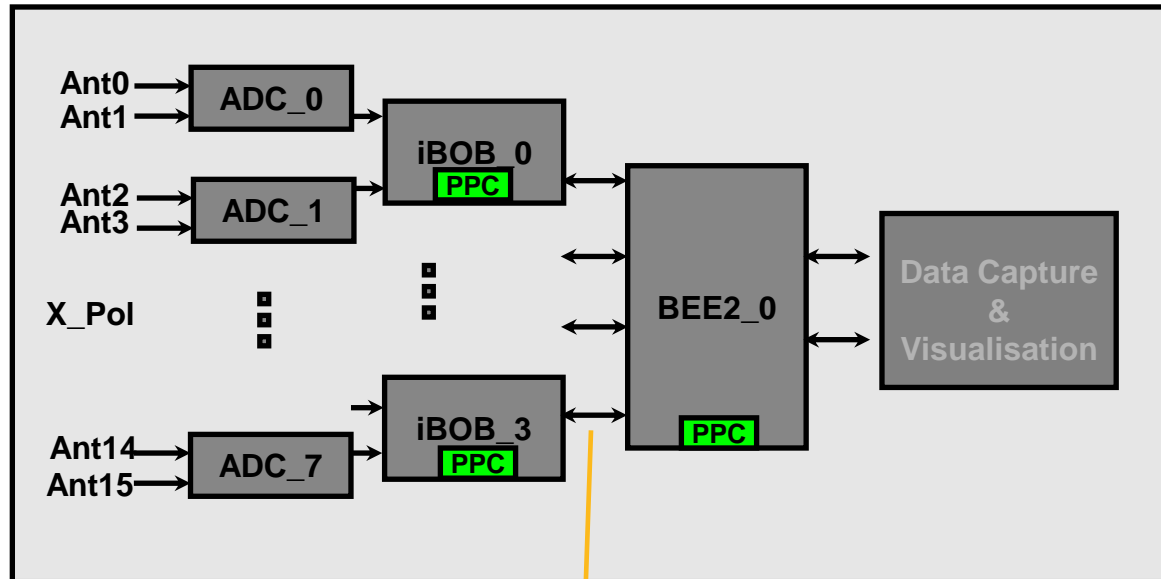


Uncalibrated





The Bandwidth problem



**32bit / clock
(max 10Gb/s)**

7 bit counter	sync	12 bit real	12 bit imag
---------------	------	-------------	-------------

Hierarchical Beamforming: The Bandwidth problem

Solution 1: Upgrade Hardware

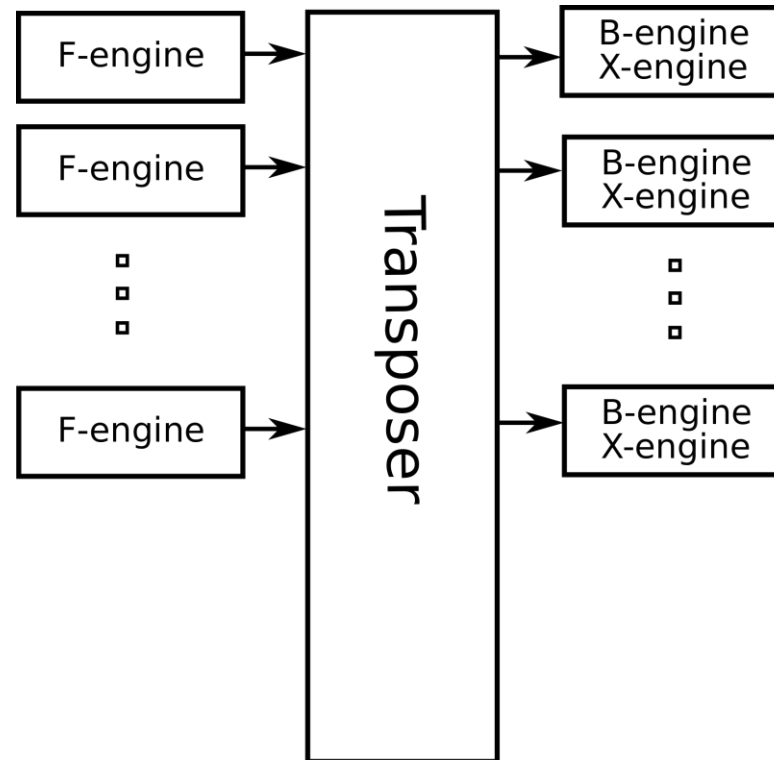


4 x 10GbE outputs

**Virtex 5: Approx 2x
DSP resources of VIIP**

Hierarchical Beamforming: The Bandwidth problem

Solution 2: Change Architecture





2PAD is a modular test bed

It is *OBVIOUSLY* not a mini-SKA!

Currently have digital beams, can now begin playing:

- 1st stage analogue beamforming? (cf EMBRACE)**
- New Beamforming/Calibration Architectures/Algorithms**
- New digital hardware – Custom FPGA boards/ASIC**
- Something else...?**



The Balance of Power...

SKA demands $< 1\text{W}$ per signal chain

2PAD: $>5\text{W}$ (Digital only)

2PAD: 500mW for ADC (inc. interface)

High speed I/O is a significant power consumer
(and does not follow Moore's Law)

